MIXED SIGNAL MSC CIRCUIT DESIGN

Technische Universität Berlin

A Divider-less Automatic Frequency Calibration for Millimeter-Wave Sub-Sampling Phase-Locked Loop

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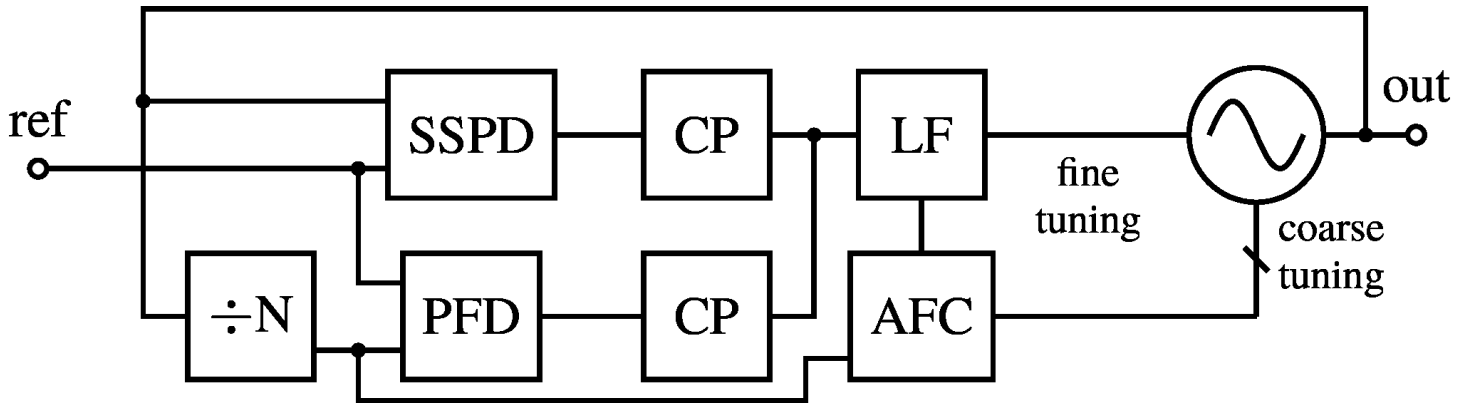
System Introduction and Problem Statement

- Sub-sampling phase-locked Loop for best jitter performance

  No multiplication of the loop noise by N^2 due to lack of frequency divider

- Sub-sampling phase detector has limited lock-in range and can not distinguish between integer multiples of the reference frequency
- SSPLLs employ secondary charge pump PLL to ensure proper locking



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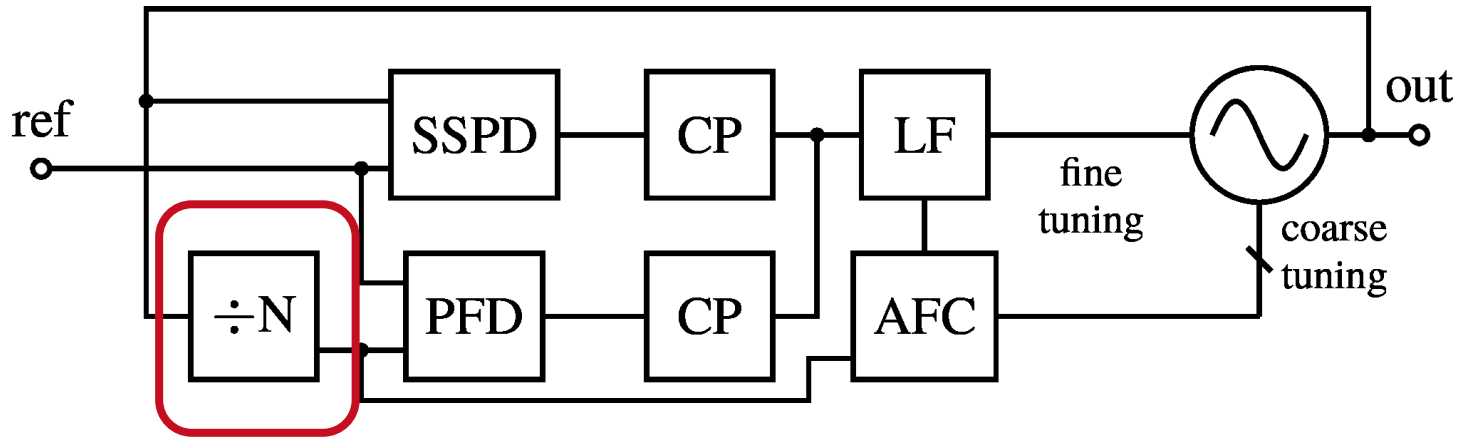
- Divider for mmw frequencies (usually CML or IL) is power hungry and large in area
- Divider-less approach desirable for high-performance mmw SSPLLs



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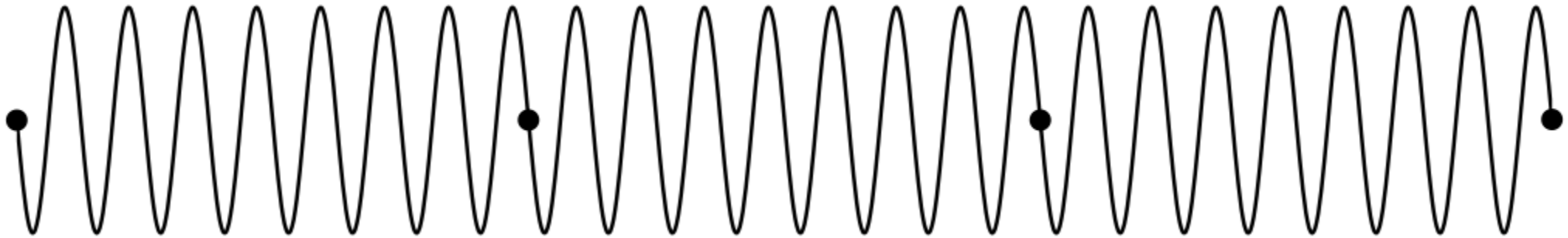

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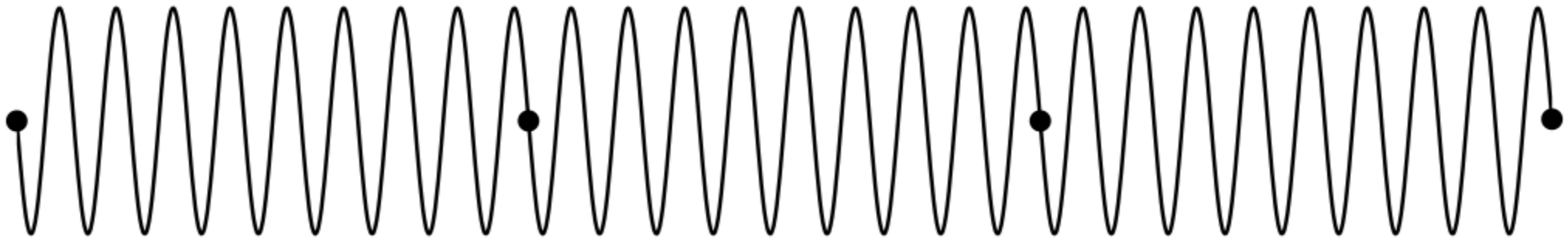

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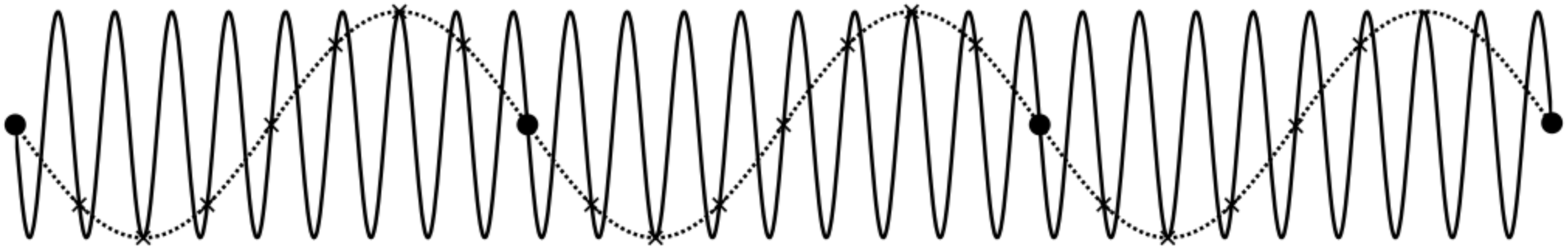

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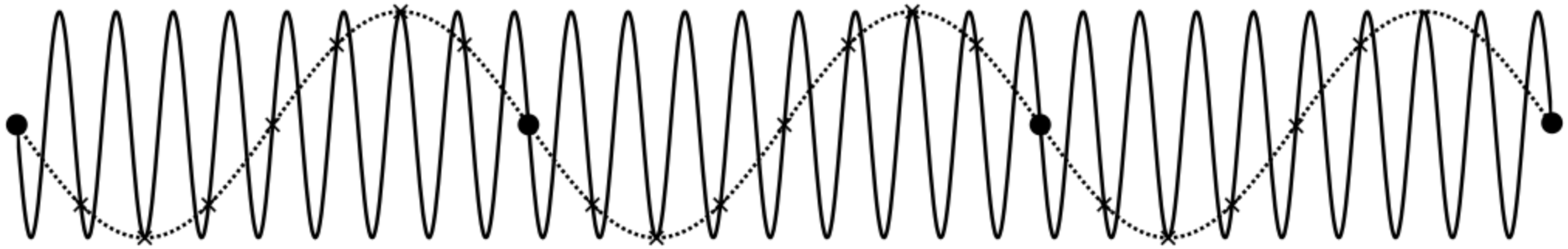

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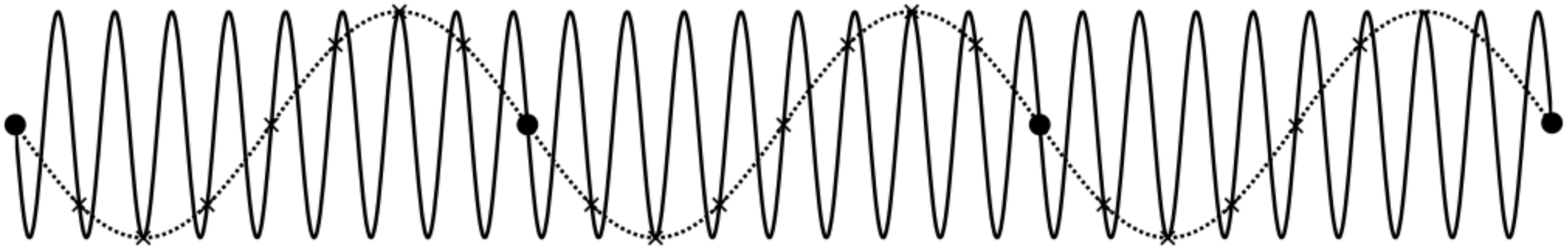

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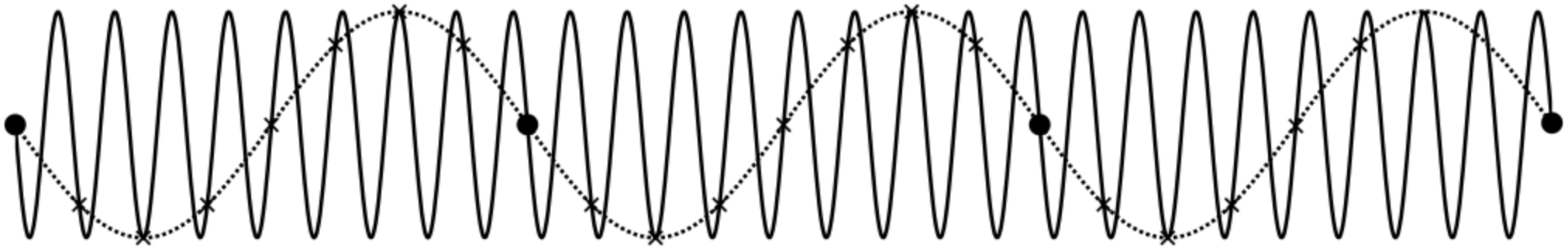

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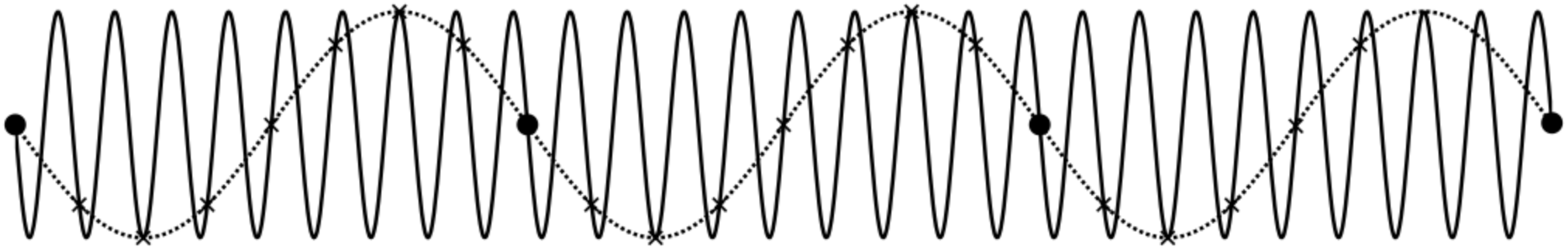
-> solve numerically for N_{aux}



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- Slightly higher detection time, but this is negligible

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- Delay PLL reference with delay-locked loop
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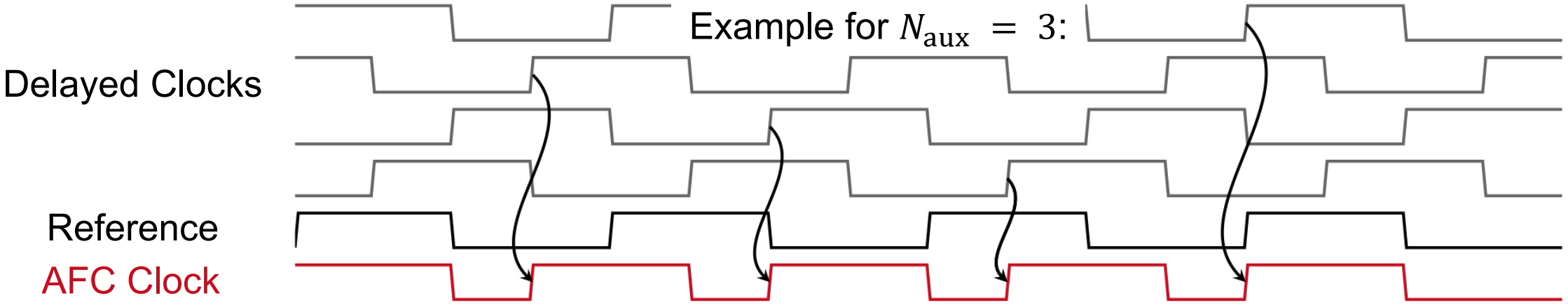
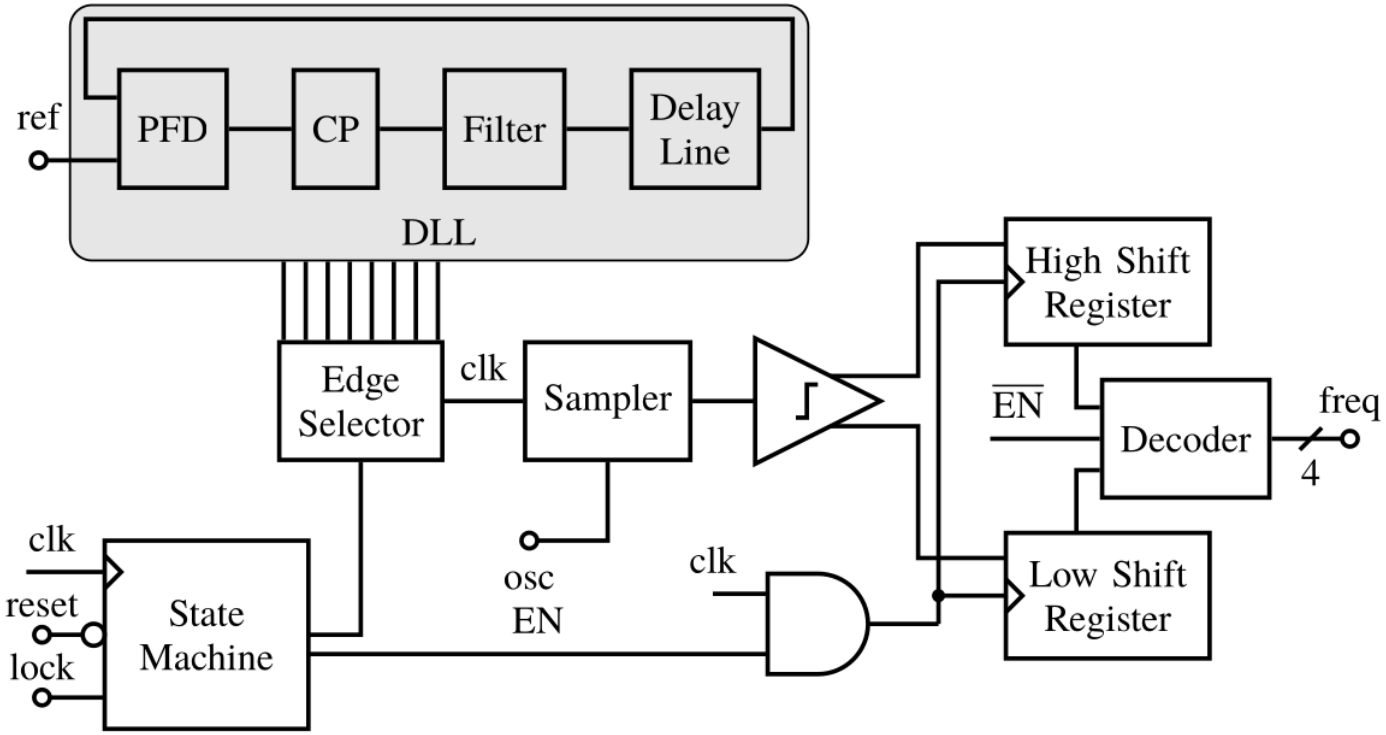


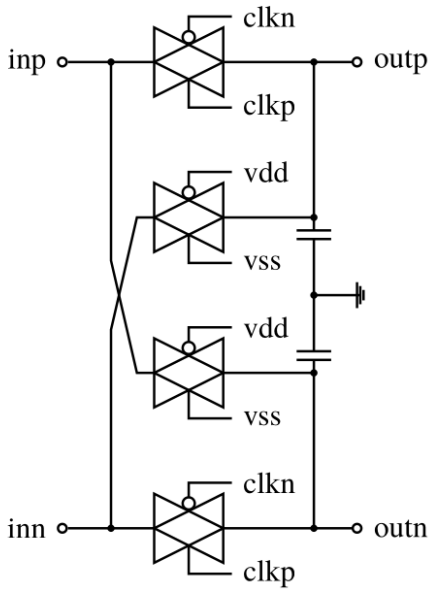
System Overview

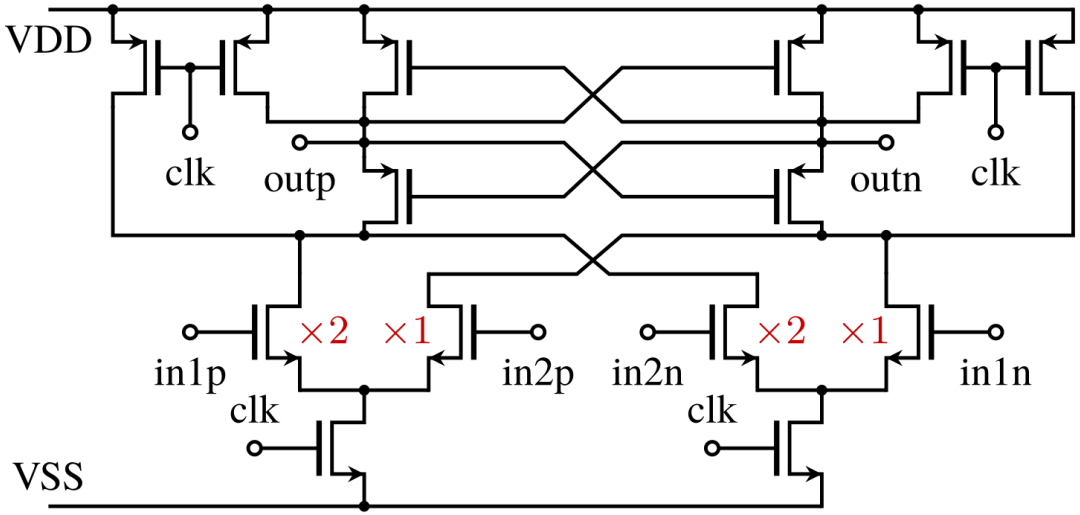
- Directly sample VCO without divider to determine frequency state
- Convert to digital representation (high, low, zero -> HHH0LLL)
- Decode frequency state and update coarse oscillator tuning
- Delayed clocks generated by a DLL and an edge selector
- High-speed sampler for VCO
- “2-Bit-ADC”: Window comparator
- Shift register and frequency state decoder
- Finite state machine controls AFC



Sampler and Comparator

- Fully-differential sampler: transmission gate as switch
- Cross-coupling between positive and negative nodes to cancel signal feedthrough during the hold phase
- Window comparator with two fully-differential comparators (strongARM latches)
- Symmetric design cancels charge injection, voltage droop etc.
- Deliberate offset (approximately 150 mV) by transistor sizing for improved noise margin and timing errors





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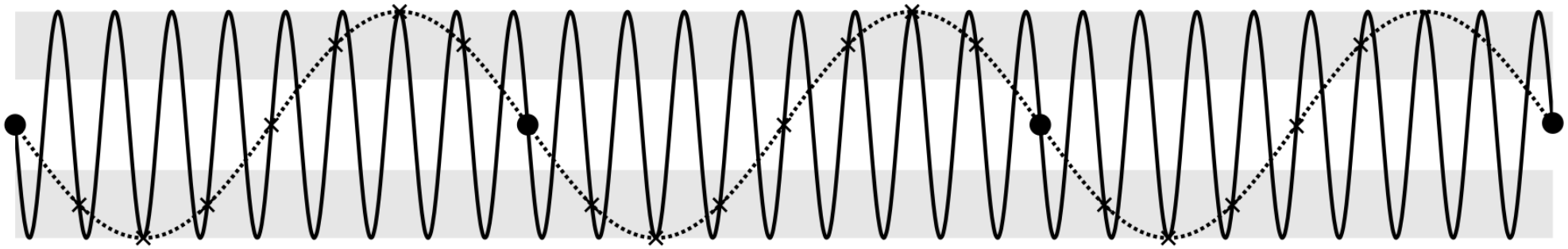
- Decoder is implemented as lookup table (simple combinatorial logic)
- Map patterns such as 0LLL0HHH0LLL0HHH to frequency state (e.g. -1)



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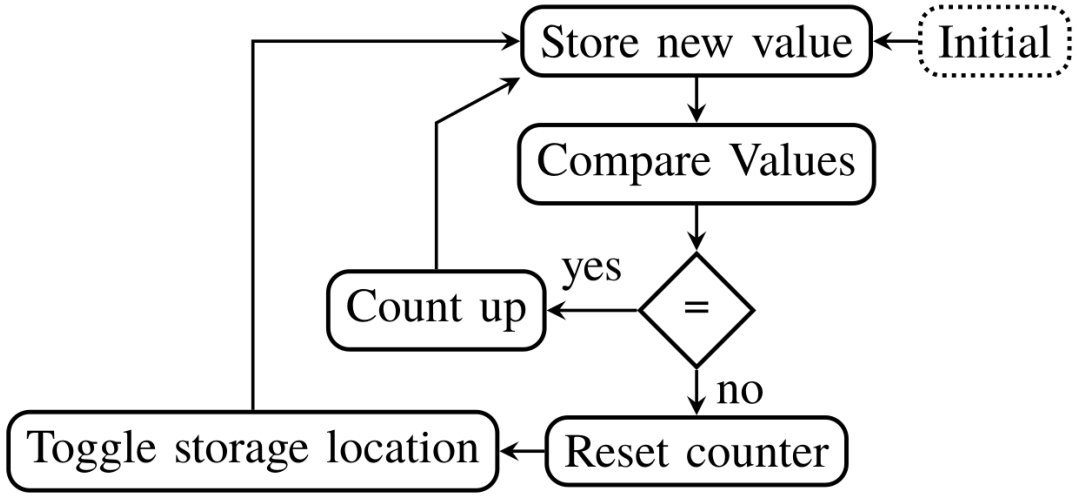

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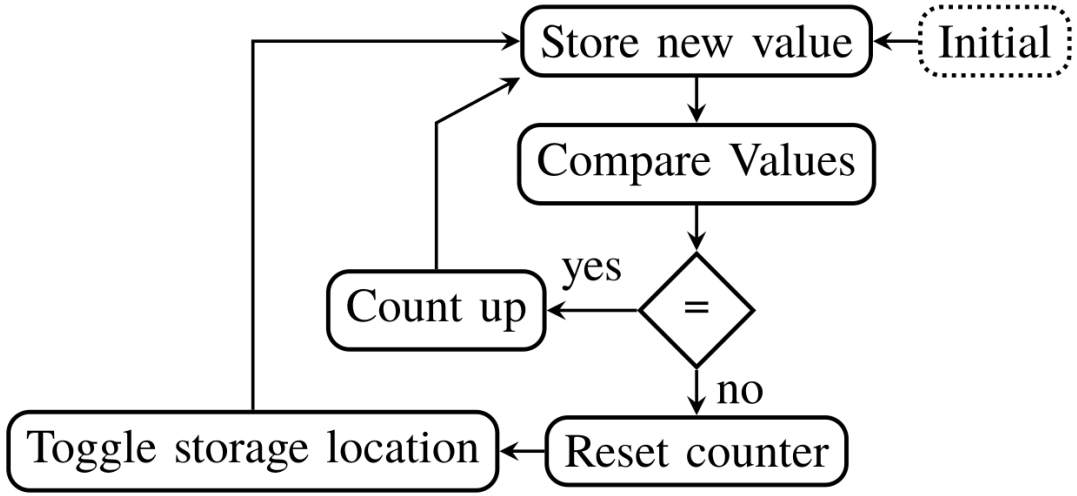

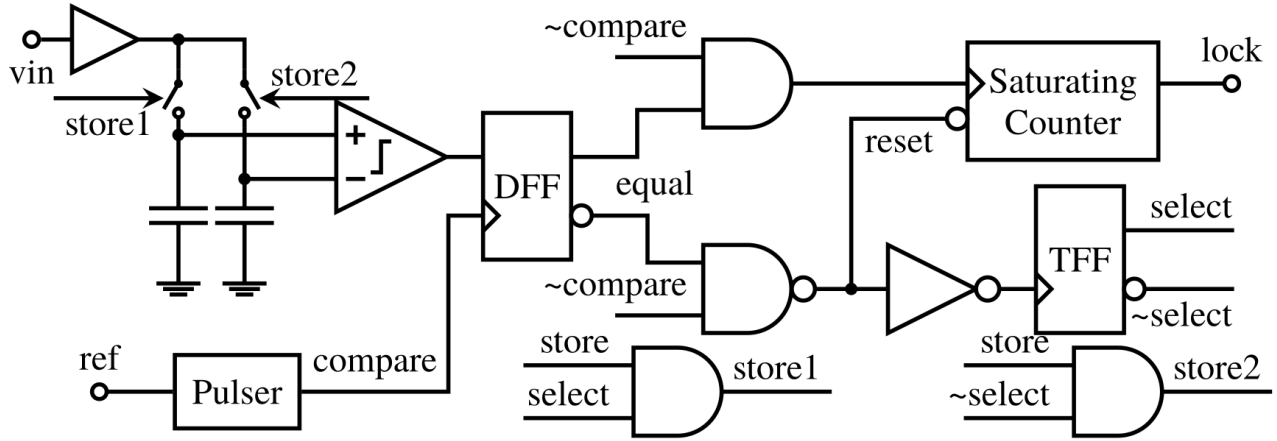

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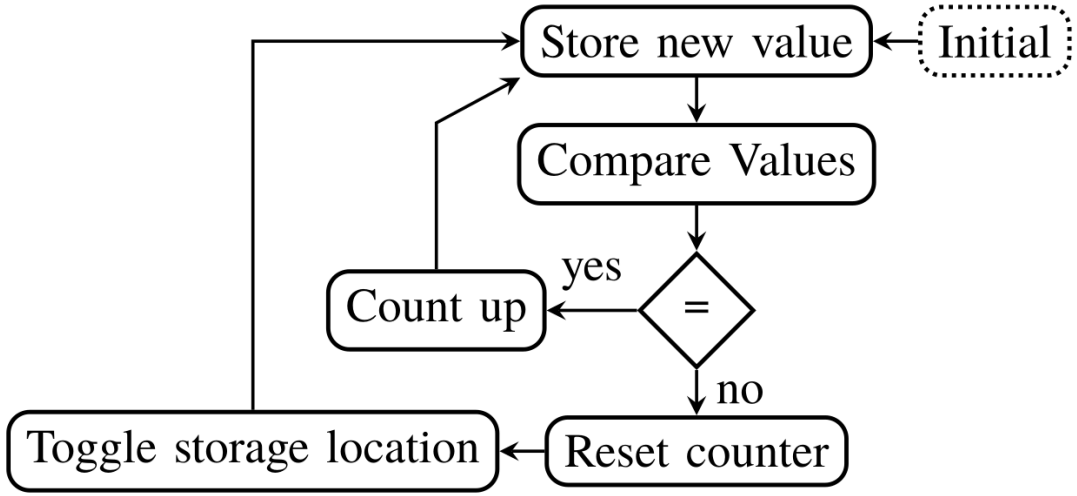
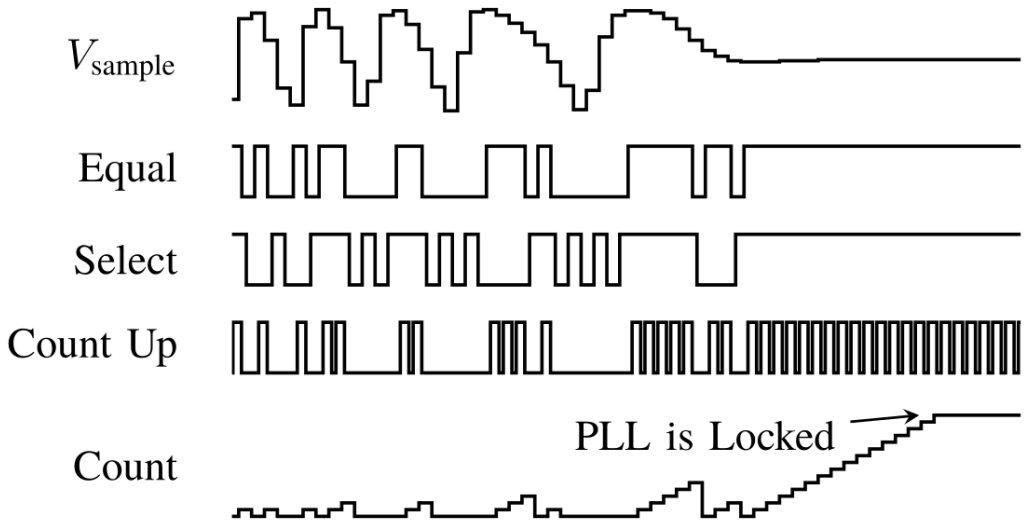
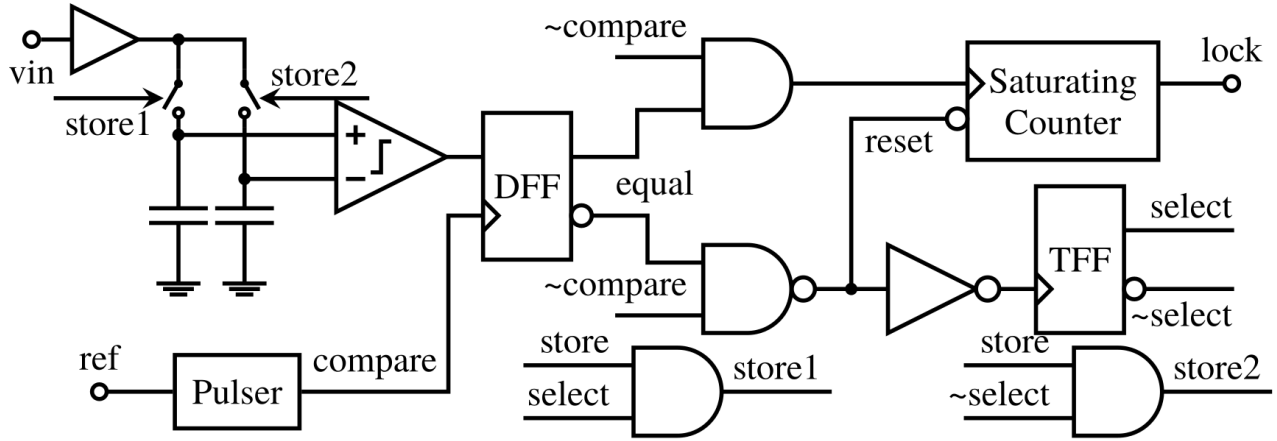
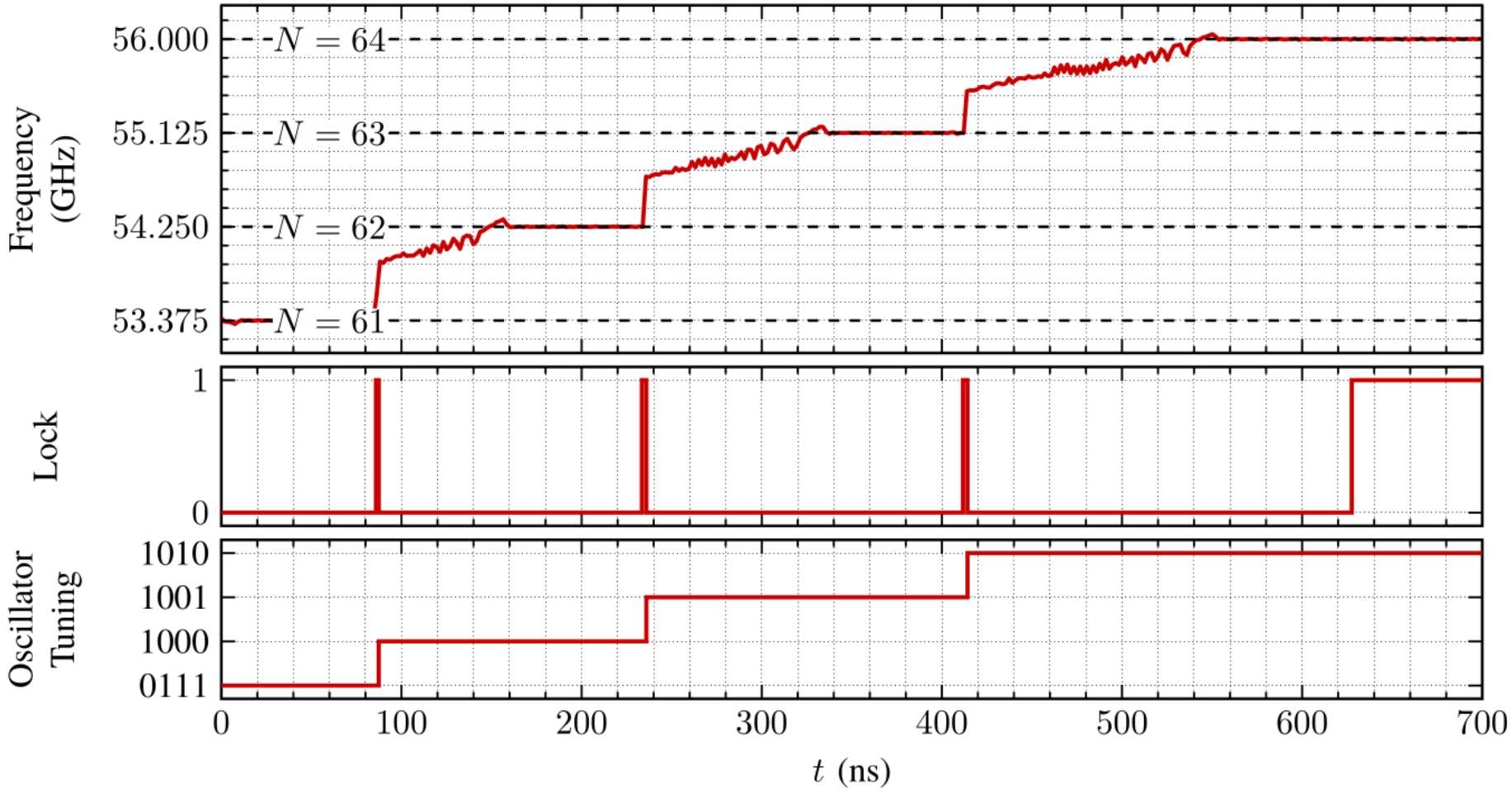






Automatic Frequency Calibration – Simulation Results

- SSPLL with $f_{\mathrm{ref}} = 875\ \mathrm{MHz}$, $f_{\mathrm{out}} = 56\ \mathrm{GHz}$ $(N = 64)$



Comparison with State-of-the-Art

Work	[1]	[7]	[8]	This work
Technology (nm)	40	180	65	22 (FDSOI)
Frequency (GHz)	14	2.3	40.5	56
Reference Frequency (GHz)	200	48	100	875
Methodology	FLL	FLL + Counter	Secondary PLL	Sub-sampling with DLL
FLL/AFC DC Power (mW)	1.5	46.7$^{\$}$	4.59	1.1
Divider	$\div$ 70	$\div$ 2	none	none
AFC/FLL Area (μm^2)	8600*	35 600*	33 600*	2000$^{\#}$

$^{\$}$ Total PLL power consumption * Estimated from die photograph $^{\#}$ Pre-layout estimation

[1] Z. Zhang *et al.*, "A 0.65-V 12-16-GHz Sub-Sampling PLL with 56.4-fsrms Integrated Jitter and -256.4-dB FoM", *IEEE Journal of Solid-State Circuits*, vol. 55, no. 6, pp. 1665—1683, 2020.

[7] W. Chang *et al.*, "A Fractional-N Divider-Less Phase-Locked Loop With a Subsampling Phase Detector," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2964–2975, 2014.

[8] Wang, Hao *et al.*, "Low-Power and Low-Noise Millimeter-Wave SSPLL With Subsampling Lock Detector for Automatic Dividerless Frequency Acquisition," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 469–481, 2021.

Conclusion

- Divider-less automatic frequency calibration for sub-sampling phase locked loops
- Suitable for highest frequencies, enables truly divider-less millimeter-wave SSPLLs
- Mainly digital implementation -> synthesizable and scalable with technology advances
- System can be extremely low power and area
- Analog front-end: Sampler, Comparator and DLL; Only sampler needs to have high speed/bandwidth
- Serialized sampling greatly reduces complexity of analog front-end
- Implementation independent of internal PLL architecture (analog, digital, discrete-time) as well as VCO type (LC, ring, etc.)
- AFC can run continuously without significantly impairing power consumption

Thank you for your Attention.
Questions?