A Divider-less Automatic Frequency Calibration for Millimeter-Wave Sub-Sampling Phase-Locked Loops

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***Abstract*—This paper presents a novel divider-less scheme for automatic frequency calibration (AFC) of sub-sampling phase-locked loops. The proposed system works without any frequency dividers at all by utilizing the phase information provided by serialized frequency detection through a sub-sampling phase detector. The detector is driven by evenly-spaced reference signals, which enables frequency detection and correction. The AFC is accompanied by a novel divider-less lock detector, which is also sample-based. The proposed system is configured to detect and correct all possible lock frequencies within the oscillator tuning range and is built, apart from the analog front-end, only with synthesizable standard cell CMOS logic.**

***Index Terms*—SSPLL, AFC, Divider-less, Lock Detector**

I. Introduction

Sub-sampling phase-locked loops (SSPLL) enable PLLs with ultra-low-jitter [1] due to their inherent feature of not multiplying the loop noise by N^2 (N = ratio between input and output frequency) [2]. This works by exploiting signal aliasing of the output signal by using a track-and-hold circuit (T&H) with the reference signal as clock. While this produces excellent phase noise results, the sub-sampling phase detector (SSPD) can not distinguish between any integer multiples of the reference frequency, hence the PLL can "false lock" to an undesired frequency. To solve this issue, typically a secondary modified type-II charge pump PLL as shown in Fig. 1 is employed [1]–[3], which only detects frequency and helps the core PLL lock to the correct frequency. As this secondary PLL uses a modified phase-frequency detector (PFD) clocked with the reference frequency, the oscillator signal needs to be divided down to the reference frequency. At millimeter-wave (mmw) frequencies, these dividers (e.g. injection-locked, current-mode-logic) are a challenge to design and have high power and area consumption [4]. In theory, the frequency-detection path could be disabled after a true lock, but this is an unreliable solution due to possible lock loss with varying temperature or voltage variations. Furthermore, high-frequency dividers are analog circuits, often relying on bandwidth enhancements through inductors, which do not scale well with technology.

To circumvent these challenges, we propose a novel divider-less frequency-acquisition scheme for SSPLLs which is based on sequential logic and therefore easy to develop and synthesizable. This enables SSPLLs to be built entirely without frequency dividers and secondary PLLs. Furthermore, the proposed system scales well with technology advancements. The used SSPLL is designed for an output frequency of 56 GHz with a reference frequency of 875 MHz. This serves as demonstration of the novel AFC, but the principle can be employed for any SSPLL.

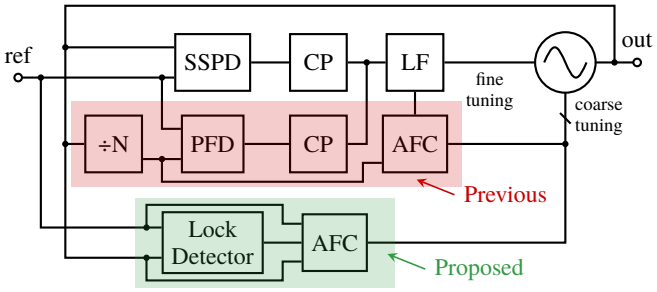

Fig. 1: System architecture of an SSPLL with a secondary charge-pump PLL (red) for frequency acquisition and the proposed AFC (green)

This paper is organized as follows: First the general principle of the frequency-acquisition scheme is described in section II. Following that, in section III the actual implementation is discussed alongside with practical improvements and simplifications. The simulation results are shown in section IV, the proposed work is concluded in section V.

II. Principle

Once a SSPLL is in lock, the SSPD samples the oscillator signal at exactly the zero crossings. In this state, the output signal of the oscillator looks like a constant voltage after the phase detector. If more than one sampler is used with equidistant sampling points, the voltage after all samplers will not be necessarily constant. This depends on the specific ratio between the input and the output frequency. Using more than one sampler can be seen as increasing the effective Nyquist frequency $f_{\mathrm{ref,eff}}$, although the reference frequency stays the same. If the output frequency is an integer multiple of $f_{\mathrm{ref,eff}}$, the SSPLL is in true lock. Otherwise, some of the samples will not lie at the zero crossings, producing characteristic patterns, depending on the lock frequency. Fig. 2 shows an example for a PLL with $N = 8$ with a true lock (8 GHz) and several false locks. The reference frequency is 1 GHz, 7 auxiliary samplers are used. This leads to an effective sampling frequency of 8 GHz. In the case of the true lock, all sampling points occur at the zero crossings, while in false lock the output frequency is aliased to some non-zero frequency.

This property can be used to find the state the PLL has locked in. In lock (true or false), the output frequency of

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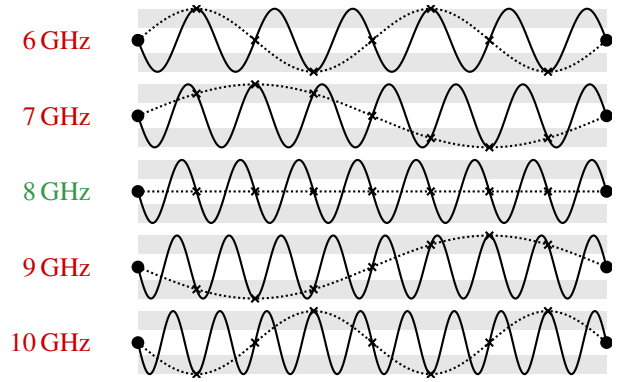

Fig. 2: Sampling of the oscillator signal at equidistant time points for different possible PLL lock frequencies (locking to the falling edge). The dots represent the main SSPD sampling points, the crosses are the samples of the auxiliary samplers. The shaded areas mark the different windows of the comparator.

the PLL will always be an integer multiple of the reference frequency. Therefore, the number of auxiliary samplers N_{aux} must be chosen in order to create non-DC signals for all possible integer multiples of the reference frequency within the frequency range of the oscillator. Additionally, the pattern captured by the auxiliary samplers in true lock should be unique to distinguish true from false lock. The simplest solution is to make sure that the effective reference frequency $f_{\text{ref,eff}}$ is an integer divisor of the oscillator output frequency. With these two constraints for the minimum number of auxiliary samplers can be calculated: In false lock, the time distance between the sample points must not fit any integer multiple of half of the period of the oscillator signal and in true lock all samplers must sample the same constant voltage:

$$\frac{1}{f_{\text{ref}} \cdot (N_{\text{aux}} + 1)} \begin{cases} \neq k \cdot 1/(2 \cdot f_{\text{lock}}) \\ = k \cdot 1/(2 \cdot N \cdot f_{\text{ref}}) \end{cases} \tag{1}$$

Here, k is a positive integer, f_{lock} is any frequency the PLL can lock to, which means only integer multiples of f_{ref} within the oscillator frequency range. With the oscillator center frequency f_0 and the maximum (one-sided) tuning range Δf the PLL output frequency in lock can be expressed as:

$$f_{\text{lock}} = (N \pm i) \cdot f_{\text{ref}} \quad \text{with } i \in \left\{1, \ldots, \left\lceil \frac{\Delta f}{f_{\text{ref}}} \right\rceil \right\} \tag{2}$$

This allows to rewrite (1) as:

$$\frac{2(N \pm i)}{N_{\text{aux}} + 1} \begin{cases} \neq k & \text{for } i \neq 0 \\ = k & \text{for } i = 0 \end{cases} \tag{3}$$

This criterion has to be checked against every possible i (see (2)), which is best done numerically. Table I shows some examples of the required number of auxiliary samplers for different PLL frequency rations and oscillator tuning ranges. The number of required sampler increases with the tuning range of the oscillator, as more possible locking frequencies exist. This still is feasible for low ratios between the input and output frequency, but for high ratios with high tuning ranges more samplers than what is reasonable to implement are needed. This problem is addressed in section III.

TABLE I: Required number of auxiliary samplers depending on the PLL factor N ($f_{\text{out}}/f_{\text{ref}}$) and the oscillator tuning range

$\Delta f/f_0$	N = 8	N = 64	N = 1000
5 %	3	15	124
10 %	3	15	124
25 %	7	63	999
50 %	15	127	1999

With the frequency information provided by the auxiliary samplers, the frequency state can be decoded. For this, the samplers are followed by window comparators which detect whether a sample is high, low or zero. For each locked frequency there is a specific and unique pattern, so the exact frequency can be derived. In Fig. 2 the comparator regions are annotated and the patterns can be seen, e.g. for 7 GHz there are three high values, one zero value and three low values. The frequency state can be directly assigned by a look-up table.

III. Implementation

In this section, the implementation of the proposed AFC is presented and the differences to the general operation principle will be highlighted. The system is shown in Fig. 3. The SSPLL is designed for a reference frequency of 875 MHz and an output frequency of 56 GHz (N = 64). The tuning range of the LC-VCO is roughly ±6 GHz, which requires 15 auxiliary samplers. The proposed AFC was implemented in a 22 nm fully-depleted silicon-on-insulator technology (FDSOI).

A. Sampler Array

The proposed AFC needs an array of N_{aux} auxiliary samplers additionally to the main sampler in the SSPD. For mmw-SSPLLs the sampling capacitance poses a serious load on the oscillator, requiring additional area- and power-consuming buffers. Especially for VCOs with wide variation ranges, a high number of auxiliary samplers are needed. Therefore, this implementation does not actually use N_{aux} physical samplers, but only one, which is controlled by a delayed reference signal with a varying delay time. This continuously shifts the sampling time point. Therefore, the entire process of the detection of the PLL frequency state is serialized, which also helps on the comparator requirements, as only one is needed. The AFC uses a shift register to store the individual comparator outputs for each sample. The serialized approach takes a longer time than a parallel detection, but this is negligible, as this is not a time-critical process. The sampling capacitance of the auxiliary sampler is kept small (5 fF), as low noise is not of importance in this case. In order to reject charge injection errors and voltage variations in the hold phase, fully-differential samplers with cross-coupling are used.

B. Comparator

The comparator follows the sampler and needs to decide whether the sampled value is high, low or zero. Therefore, a window comparator is needed. The implemented comparator

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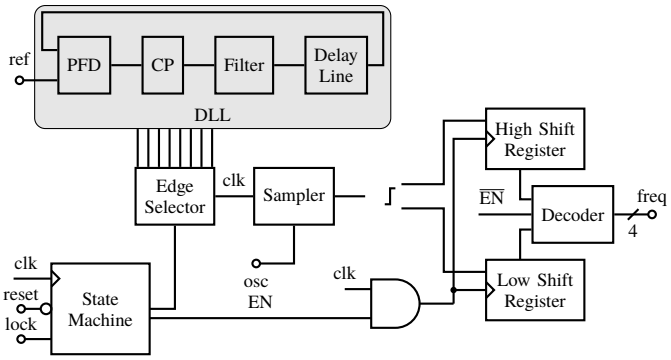

Fig. 3: AFC implementation

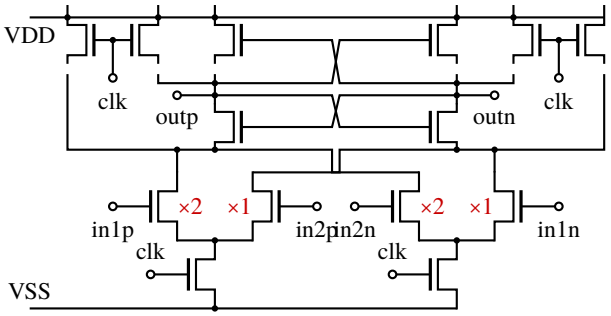

Fig. 4: Implementation of the comparator with offset. The AFC uses only one input branch (left/right) for the samples.

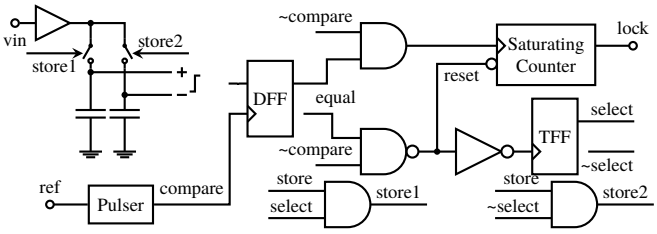

Fig. 5: Implementation of the Lock Detector

uses two fully-differential strongARM latches [5], shown in Fig. 4, for the high/low decision. The symmetric design cancels voltage droop and clock feed-through, which are quite high due to the small sampling capacitance. For greater noise margin and timing errors of the samples especially at the signal zero crossings (where the voltage change is the fastest), a deliberate offset of around 150 mV is introduced by sizing the input transistors differently (see Fig. 4). After each decision, the data is stored in two shift registers (one for each bit high/low).

C. Clock Delay and Edge Selector

The proposed AFC needs N_{aux} delayed clock signals (regardless whether the detection is serialized or not), which are provided by a delay-locked loop (DLL). The resolution of the DLL must be at least $T_{\text{ref}}/(N_{\text{aux}}+1)$. As the sampling process is serialized, a clock edge selector is needed to choose the next sampling phase. The selector cycles backwards through all clock phases, as this prevents glitches during the update of the selection signal. The inherit reordering of the samples can can simply be fixed in the decoder.

The DLL is implemented following standard design practice, comprising a PFD as well as a charge pump and a delay chain with 32 current-starved inverters delays.

D. Decoder

The decoder maps the digital output of the comparators/shift registers to a frequency state and controls the coarse tuning setting of the oscillator. In this implementation, the oscillator features a four-bit tuning word. The decoder is realized as a look-up table, where every possible state is represented. The corresponding states can be calculated from the specifics of the given PLL architecture (its output frequency, frequency range, reference frequency etc.). For example, in Fig. 2 at 7 GHz, there are three high (H), one zero (0) and three low (L) values (HHH0LLL), whereas for 10 GHz it is L0H0L0H.

In SSPLLs, the polarity of the gain of the charge pump can be negative or positive. This does not break the negative feedback, but changes whether the PLL locks to the rising or the falling edge. This also affects the detection of the state in the AFC. Fig. 2 showns a falling-edge type, for a rising edge type the values are simply mirrored around the true lock, for example 0L0H0L0H0 becomes 0H0L0H0L0.

E. Lock Detector

Contrary to a frequency correction with a PFD, where the secondary loop can run continuously, the proposed AFC must only operate while the SSPLL is locked (false or true lock). Therefore the implementation of the AFC needs a lock detector. Conventionally, a lock detector is built with digital gates [6], which cannot be operated at mmw-frequencies, therefore these lock detectors operate in the frequency-divided path. In the proposed implementation, the sampled voltage (after the SSPD) is monitored. If the SSPLL is in lock, it is constant and the proposed lock detector checks if enough consecutive samples are equal by comparing the previous and current sample by re-using the window comparator. If the values are equal, a counter is incremented. When the counter reaches a certain threshold, the SSPLL is assumed to be in lock. If on the other hand the values are different, the counter is reset and the previous value is updated by simply swapping the status of the storage location (previous ↔ current). The implementation of the lock detector is shown in Fig. 5.

An example of the lock detector waveforms is given in Fig. 6. In regions with slow voltage changes the counter starts accumulating, as there are a few consecutive values that are considered equal. However, only after the PLL is locked the counter accumulates until the lock detection flag is set. For the visualization, the final value of the counter is set to a low value, in the real implementation this value is set higher.

IV. Simulation Results

Figure 7 shows the simulated waveforms of the proposed AFC. The first graph shows the voltage after the track-and-hold in the hold phase. The second graph shows the output frequency of the PLL. There are four events where the PLL is locked (at

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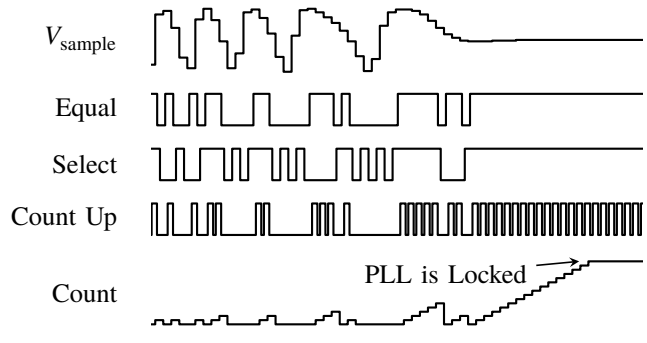

Fig. 6: Lock Detector Waveforms

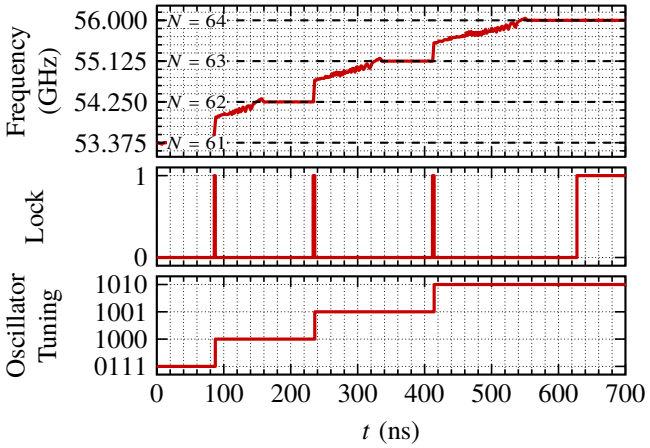

Fig. 7: Simulated signals of the SSPLL with the proposed AFC

85 ns, 235 ns, 420 ns and 630 ns). This can be seen in the output frequency and the lock detector/AFC signals. However, the first three locks are false locks. At each of these events, the lock detector correctly detects the lock, triggering the AFC. For the three false lock cases, the the digital coarse frequency setting is updated correspondingly (in these scenarios the setting is increased). As the PLL quickly loses lock, the lock detection signal is reset again. The fourth case shows then the true lock, where the lock detection signal stays set and the coarse tuning remains unchanged. The output frequency is now correct at 56 GHz and the PLL is in true lock.

V. Conclusion

This paper demonstrates the design of a divider-less circuit for automatic frequency calibration of sub-sampling phase-locked loops. Apart from the analog samplers, DLL and comparators, the system is entirely digital and synthesizable. Furthermore, only the samplers operate at the PLL output frequency, the remaining circuits are implemented for the lower reference frequency. As the system is mainly digital with small analog circuits, the area consumption can be very low, especially compared to huge inductor-based frequency dividers (bandwidth-enhanced CML or injection-locked). The proposed principle is easy to adapt to different PLL configurations (oscillator tuning range, input/output frequency ratio) and is independent of oscillator/charge pump/filter architecture (e.g. it is also applicable in digital SSPLLs). Additionally, the system can operate continuously while maintaining a low power consumption by periodically running a frequency test.

Work	[1]	[7]	[8]	This work
Technology (nm)	40	180	65	22 (FDSOI)
Frequency (GHz)	14	2.3	40.5	56
Reference Frequency (GHz)	200	48	100	875
Methodology	FLL	FLL + Counter	Secondary PLL	Sub-sampling with DLL
FLL/AFC DC Power (mW)	1.5	46.7$	4.59	1.1
Divider	÷ 70	÷ 2	none	none
AFC/FLL Area (μm^2)	8600*	35 600*	33 600*	2000#

$ Total PLL power consumption
* Estimated from die photograph # Pre-layout estimation

TABLE II: Comparison with state-of-the-art

Table II shows the comparison with the state of the art. In [7], a counter-based AFC is used, but this requires divide-by-two quadrature dividers and the PLL operates at much lower frequencies (2.3 GHz). In [8] a truly divider-less SSPLL design is presented which employs a secondary PLL for high-frequency reference generation and uses a similar principle as shown in this work. However, a significantly increased reference frequency is used, which is often not feasible, especially for two-stage PLLs. Compared to similar designs, this work provides an AFC scheme optimally suited for mmw-SSPLLs.

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