A mmw Low-Noise Sub-Sampling Phase-Locked Loop with a Non-Pulsed Charge Pump, Frequency Calibration and a Compact Ultra-High-Q Resonator

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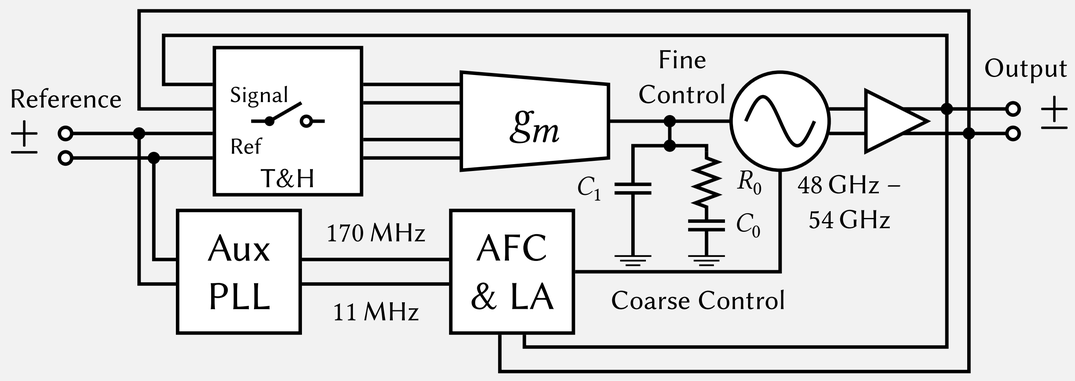
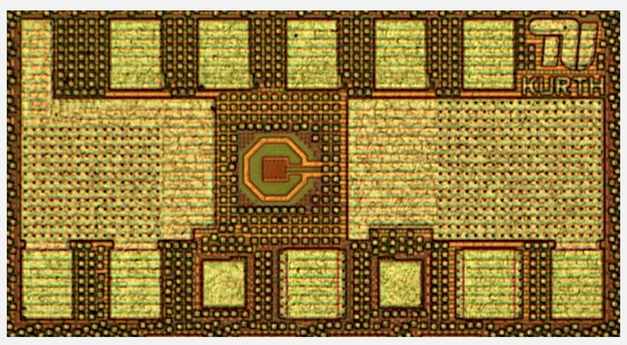
Toplevel PLL System: Sub-Sampling Phase-Locked Loop with Automatic Frequency Calibration

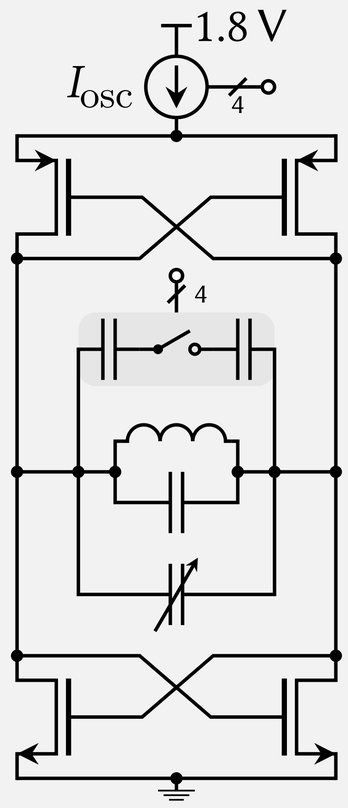
- Sub-sampling phase-locked loop with LC oscillator
- High-Q resonator with simple oscillator architecture for low power operation
- Novel double-sampling charge pump with 78 % power consumption reduction
- Divider-less digital automatic frequency calibration and lock-assist system



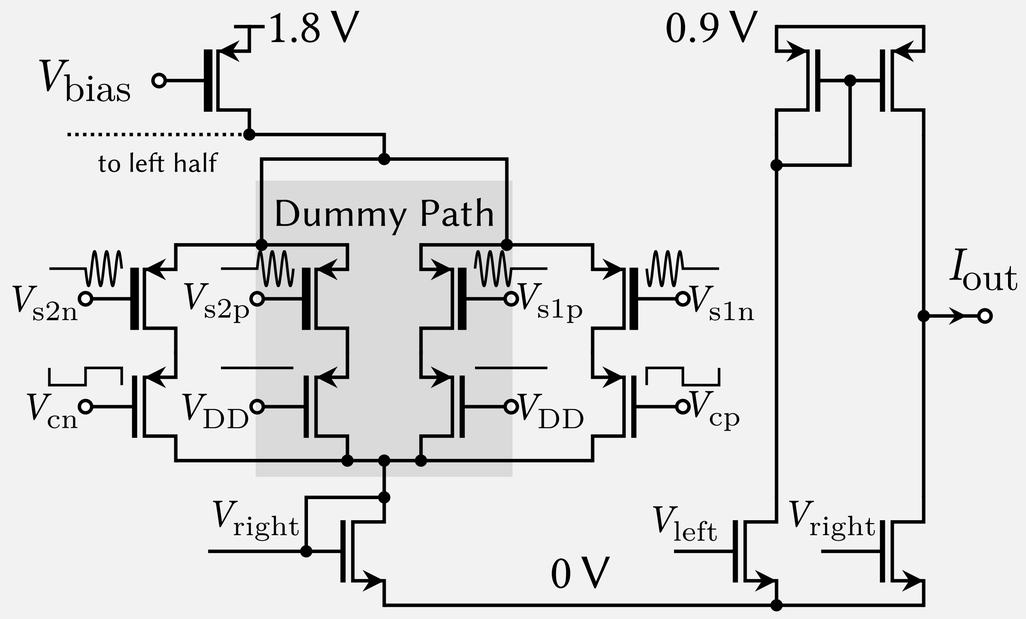
LC Oscillator

- Standard complementary architecture
- High-Q resonator with top-metal capacitor
- 4-bit coarse frequency control for calibration
- Fabricated in 22-nm-FDSOI
- Measured $\mathscr{L} = -86.5\,\mathrm{dBc/Hz}$
- P_{DC} = 4.5 mW





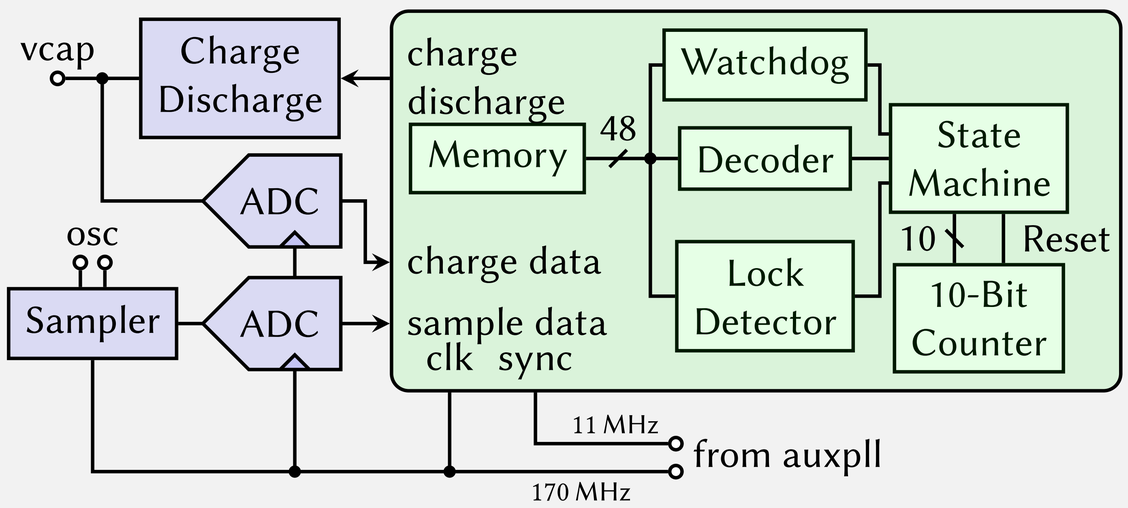
Charge Pump Implementation



- Non-switched continuous output current
- Highly reduced power consumption due to pulser-less operation
- Virtual reference frequency doubling

Frequency Calibration System

- Sub-sampling loop with different reference frequency
- Aliasing frequency chosen with respect to the VCO range
- Only one possible SSPLL output frequency for both loops
- Additional watchdog-based lock-assist with filter capacitor charging
- Monitoring of the SSPLL control voltage to avoid extreme values
- Digital implementation (green) with analog front-end (blue)



Results

- Implemented and simulated in 22-nm fully-depleted silicon-on-insulator
- Integrated measurement results from VCO
- Output phase noise at 50.75 GHz
- Characterized with system model and sub-block noise models/simulations