A mmw Low-Noise Sub-Sampling Phase-Locked Loop with a Non-Pulsed Charge Pump, Frequency Calibration and a Compact Ultra-High-Q Resonator

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***Abstract*—This paper presents the architecture and implementation of a low-noise sub-sampling phase-locked loop (SSPLL) for mm-wave frequencies. It leverages an LC oscillator with a novel resonator, a digital lock assist and frequency calibration system as well as a novel charge pump implementation. The charge pump eliminates the pulser and runs continuously, which significantly reduces its power consumption while maintaining equal noise performance. The calibration system solves the lock problem of the SSPLL by implementing a lock/frequency search to prevent non- and false-lock. The LC oscillator employs an optimized resonator which combines both the inductor and the capacitor on the same metal, resulting in a very high quality factor by eliminating the interconnect resistance within the resonator. The SSPLL was implemented and simulated in a 22-nm-FDSOI technology, alongside with measurement results of the LC oscillator, which was fabricated in the same technology.**

***Index Terms*—Sub-Sampling Phase-Locked Loop, Millimeter-Wave (mm-Wave), Frequency Calibration, Lock Assist, High-Q Resonator**

I. Introduction

In recent years, data rates of communication systems have increased tremendously, leading to the development of high-performance digital transceivers with fast analog/digital converters (ADC/DAC) with high resolution. Their operation requires phase-locked loops with ultra-low phase noise for the generation of carrier signals and clocks, which raises the overall power consumption significantly. Sub-sampling phase-locked loops (SSPLLs) offer lowest phase noise with high power efficiency and can be easily integrated and built in CMOS [1]. Therefore, they are ideal candidates for clock/carrier generation in high-performance transceiver systems. Nonetheless, SSPLLs have a few issues compared to typical type-II charge-pump-PLLs (CPPLLs): They suffer from limited lock-in range and have the possibility of false frequency locking (due to aliasing). Various solutions for these issues exist (e.g [2], [3]), which introduce higher complexity and do not solve all lock issues.

In this paper, a SSPLL for mm-wave frequencies is presented, which addresses common issues and exhibits a high power efficiency and low phase noise. These key points are achieved by a optimized LC oscillator with a special combined high-Q resonator, a novel charge pump (CP) which runs continuously and offers significantly reduced power consumption and supply current ripple as well as a digital automatic frequency calibration with minimal analog front-end, preventing false locking and helping the SSPLL to lock. The work is organized as follows: In section II the overall system architecture is shown, with subsections for all important sub-circuits of the loop. The oscillator is described in its own section III as it builds on a specialized design and includes measurement results. The frequency calibration system is described in section IV. The simulation results of the entire system, including incorporation of the measured results from the oscillator, are discussed in section V. Finally, the paper is concluded in section VI.

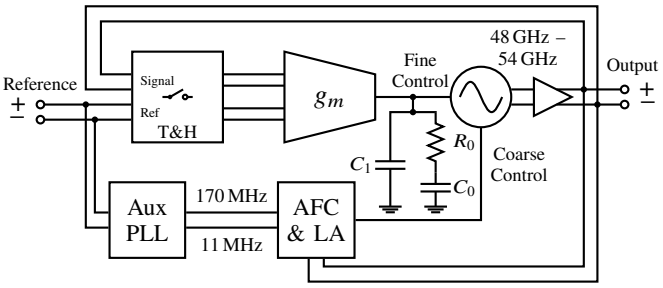

Fig. 1: System Architecture of the Sub-Sampling Phase-Locked Loop including the main phase control loop and the frequency calibration/lock assist (AFC & LA) with auxiliary PLL

II. System Architecture

Figure 1 shows the overall system architecture of the proposed sub-sampling phase-locked loop. It is a type-II SSPLL with a differential sampler, a novel non-pulsed charge pump and a LC oscillator with an optimized high-Q resonator. For automatic frequency calibration (AFC) and lock assist (LA), a sub-system is implemented that continuously monitors the lock state of the SSPLL. This sub-system requires additional low-frequency clock signals with a specific frequency relation to the main reference signal (see IV), therefore a simple low-frequency type-II CPPLL is also included. The AFC+LA sub-system alleviates locking issues as limited pull-in range and prevents false locking to a wrong frequency, which would be possible otherwise due to aliasing.

A. Frequency Concept and Loop Transfer Function

The SSPLL is designed for an output frequency between 50 GHz and 60 GHz. A reference frequency of 875 MHz is chosen, due to the availability of high-frequency crystal

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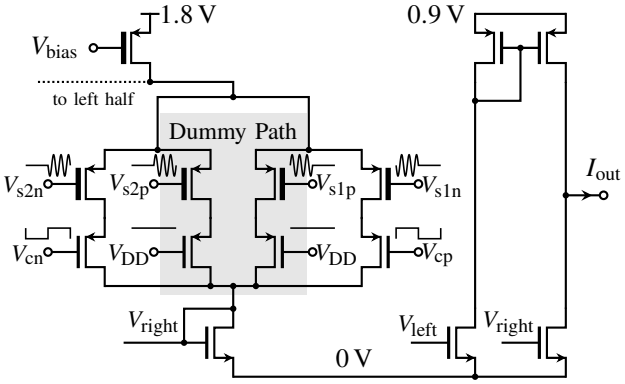

Fig. 2: Implementation of the Charge Pump (right half)

oscillator modules. In a possible future two-stage concept, this frequency can be synthesized on-chip. The high reference frequency allows for a high loop bandwidth, which can be beneficial for the phase noise performance of the entire SSPLL. With this, a loop bandwidth of roughly 50 MHz is chosen.

From the loop bandwidth (typically a maximum of $f_{ref}/10$ is considered, although lower values are possible too) and the measured tuning curve of the oscillator (and the corresponding oscillator gain $K_{VCO} \approx 1.1\,\mathrm{GHz/V}$), the loop dynamic are established by the filter with the following values [4]:

$$R_0 = 1\,\mathrm{k\Omega} \qquad C_0 = 100\,\mathrm{pF} \qquad C_1 = 1\,\mathrm{pF}$$

B. Charge Pump

Figure 2 shows the implementation of the charge pump (only half of the front-end is depicted). In contrast to typical CP implementations that employ a pulser to enable the output only during the hold phase of the phase detector, the proposed implementation does not require a pulser and hence runs continuously. This has two advantages: It reduces the current ripple at the output and it greatly reduces the power consumption of the charge pump, since the pulser has a major impact. This is due to the typical implementation of the pulser: a chain of CMOS inverters is used to add delay to the clock signal. After the chain, the delayed and the original clock signal are combined by an AND-gate. Compared to the charge pump core, this inverter chain draws significantly more current and uses more active circuit area [5]. Furthermore, this charge pump implementation uses both differential samples from the phase detector, which is usually not done in the conventional implementation, as the pulser enables the charge pump only during the hold phase of one sampler. This leads to a virtual reference frequency doubling without changing the bandwidth requirements of reference buffers, sample switches etc. The proposed charge pump design exhibits the same noise performance as an comparable conventional design and is additionally also more area efficient, due to the lack of a pulser. Duty-cycle issues of the clock do not impair the function of the charge pump, as it operates on samples that are obtained with the same clock and are therefore subject to the same imperfections.

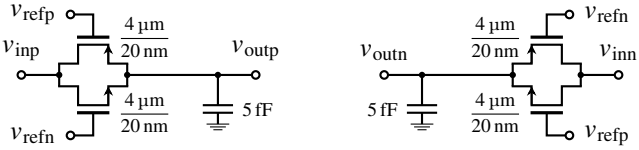

Fig. 3: Implementation of the sub-sampling phase detector

The implementation of the novel charge pump employs two differential input pairs (four inputs in total) for the four different signals coming from the phase detector operating in a ping-pong fashion. The current branches are enabled when the input signal is in the hold phase. The currents are summed into a diode-connected transistor to produce the bias voltage for the output current mirror. On both sides of the input the voltage is generated, leading to a continuous biasing of the output current mirror. With this, the switches at the output can be eliminated and moved to the input.

The dummy path that is shown in figure 2 reduces the signal feed-through of the input signal during the track phase. This works by adding additional always-off paths which amplify the inverse signal. This cancels the feed-through onto the gate nodes of the diode-connected transistors (only limited by mismatch).

C. Sub-Sampling Phase Detector (SSPD)

The SSPD is implemented with transmission gates in order to minimize resistance variation of the entire signal range. Furthermore, differential operation is essential to increase robustness against charge injection as well as signal feed-through. The latter issue can be optimized further by employing cross-coupling with always-off switches. The sampling capacitance can be as low as 5 fF, as the sampled noise in SSPLLs due to the phase detector usually is not an issue [1]. The implementation of the SSPD is shown in figure 3.

III. Oscillator

Figure 4 shows the circuit implementation of the LC oscillator. At its core, a novel resonator – optimized for a high quality factor Q – enables low phase noise and high power efficiency with this comparably simple design. The frequency-defining capacitance is divided into a fixed and a variable part, where the former is integrated together with the inductor on the same metal. This eliminates the interconnect resistance coming from vias between higher and lower metals [6].

Typically, capacitors in integrated circuits are implemented in lower metal layers, which offer high density and therefore also high capacitance density. However, the height of higher metals is increased, which leads to higher fringe capacitance between the fingers of a metal-oxide-metal capacitor. In the used technology, the capacitance density can reach $100\,\mathrm{aF/\mu m^2}$. With a target capacitance of approximately 35 fF a capacitor with an area of $20\,\mu\mathrm{m} \times 20\,\mu\mathrm{m}$ is required. This capacitor fits into an inductor with an inductance of 150 pH. The electro-magnetical simulation of this structure shows expected resonator behavior, with a Q-factor-improvement of 38 % over a comparable conventional LC resonator.

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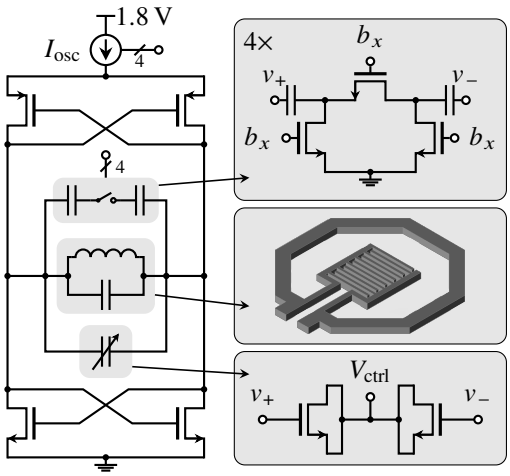

Fig. 4: Top-level Circuit of the LC Oscillator

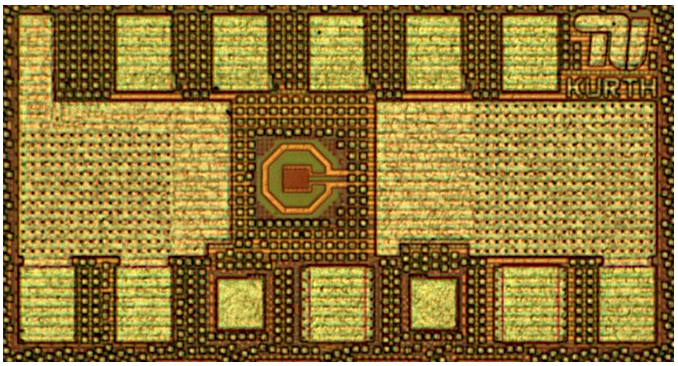

Fig. 5: Die Photograph of the LC Oscillator

The LC oscillator was fabricated in a 22-nm-fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. Figure 5 shows the die photograph of the LC oscillator. The entire circuit (except for pads and their connecting wires) together with serial interface for calibration and pad driver occupies $0.013\,\mathrm{mm}^2$, whereas the oscillator core including resonator takes up only $0.007\,\mathrm{mm}^2$. The optimized resonator with the integrated fixed capacitance can be clearly seen inside of the inductor. The circuit was measured as a bare die on a wafer prober. The differential oscillator output signal was probed by a PGSGSGP probe, which includes DC power pins on the left and right side, therefore seven probe pads can be seen on the lower part of the circuit. The the oscillator was tuned via a serial interface, whose control pins are on the top.

The spectrum and phase noise of the oscillator were measured with a Rohde & Schwarz FSW67 spectrum analyzer and are shown in figure 6. For the measurement, a balanced-unbalanced converter (balun) was used for differential-to-single-ended conversion. This balun together with the cables etc. attenuates the signal by more than 26 dB, which leads to a low received signal power of −50 dBm. The oscillator shows an excellent phase noise performance of −86.5 dBc/Hz at an offset frequency of 1 MHz. The power consumption is 4.5 mW, which relates to a Figure-of-Merit (FoM) of −175 dBc/Hz.

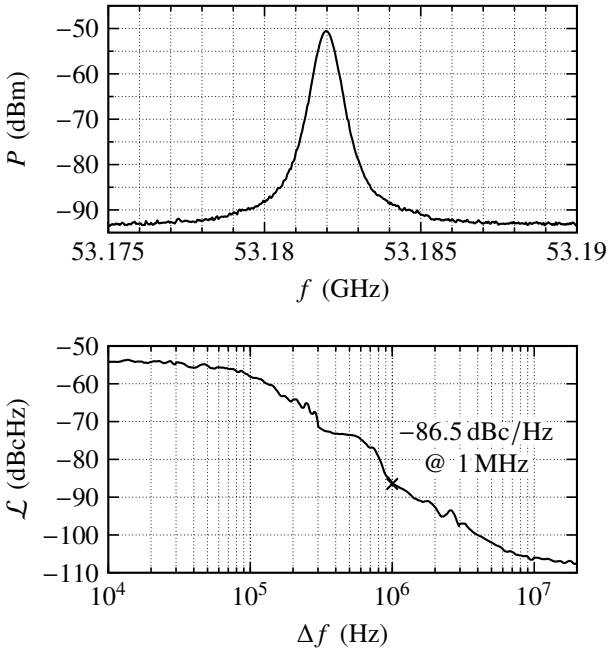

Fig. 6: Measured Spectrum (top) and Phase Noise (bottom) of the LC Oscillator. RBW = 500 kHz (power) / 10 % (phase noise), VBW = 500 kHz, Attenuation = 0 dB

IV. Lock Assist and Frequency Calibration

A sub-sampling phase-locked loop achieves phase lock by aliasing the oscillator frequency to 0 Hz. This is done by sub-sampling the oscillator signal with the reference signal and make the SSPLL lock to an integer multiple of the reference. However, it is not possible to distinguish between the correct multiple and any other possible frequency within the tuning range of the oscillator. Furthermore, as the sub-sampling phase detector can not detect frequency (as opposed to a conventional phase-frequency detector – PFD), the SSPLL suffers from all typical locking limitations as other non-PFD PLLs. Therefore two issues arise in SSPLLs: Not locking at all and locking to the wrong frequency. In this work, we demonstrate a frequency calibration and lock assist sub-system for sub-sampling phase-locked loops that eliminates both these issues. The overview is shown in Figure 7 [7]. All signal processing is done digitally, making this approach robust. Only the front-end is implemented with low resolution analog-to-digital converters, a simple charge/discharge circuit (a switched current mirror) and a replica of the main sampler (the phase detector of the SSPLL).

For the false-lock detection, the oscillator is sampled with a replica of the main sub-sampling phase detector, but at a different frequency. The clock signal for this sampler is generated by an auxiliary CPPLL. Its frequency has a specific fractional relation to the main reference signal. This enables aliasing the oscillator signal to a known frequency different from 0 Hz. From this frequency (or more precisely, from the samples representing it), the digital decoder can recognize the actual lock frequency, which then in turn can be corrected for.

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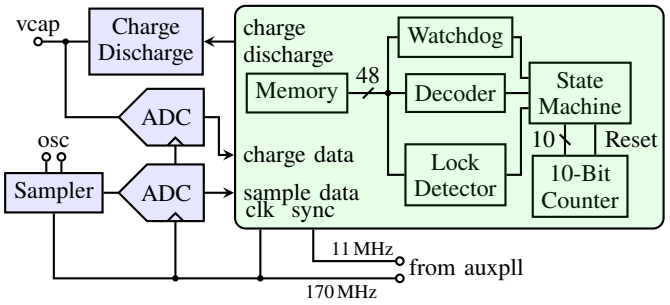

Fig. 7: Implementation of Automatic Frequency Calibration and Lock Assist; Green: Digital, Blue: Analog

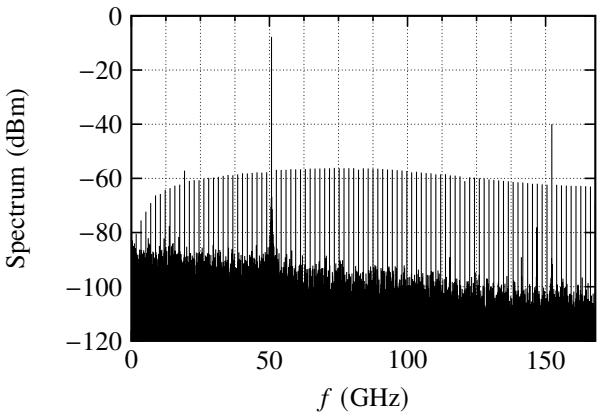

Fig. 8: Simulated output spectrum of the entire SSPLL in lock at 50.75 GHz (number of points: 1920)

V. Simulation Results

The proposed SSPLL was implemented and simulated in a 22-nm-fully-depleted-silicon-on-insulator (FDSOI) technology. For simulation, measurement results from the LC oscillator were included. Figure 8 shows the simulated output spectrum of the sub-sampling phase-locked loop when the SSPLL has locked to a frequency of 50.75 GHz. Figure 9 shows the phase noise spectrum of the sub-sampling phase-locked loop. It was calculated with a system model by characterizing the noise power spectral density of the individual sub-circuits, alongside their noise transfer function [8]. The phase noise spectrum for the oscillator was fitted from measurement results.

VI. Conclusion

In this paper a sub-sampling phase-locked loop for mm-wave frequencies was presented. The system architecture leverages several improvements over typical SSPLL implementations: The charge pump operates in a continuous fashion, as opposed to classical charge pumps in SSPLLs, which employ a pulser and operate non-continuously. This significantly reduces both the supply current ripple and the power consumption of the charge pump by roughly 87 % and 78 %, respectively. Furthermore, the phase noise and power efficiency of the entire SSPLL are improved by using a simple LC oscillator architecture with an optimized high-Q resonator. The lock frequency of the SSPLL is controlled by a low-power digital calibration system which also assists the SSPLL to lock. A comparison with other state-of-the-art PLL implementations is shown in Table I, where the proposed work shows a very competitive design. A tape-out of the entire SSPLL with the integration of the already-implemented oscillator is in preparation.

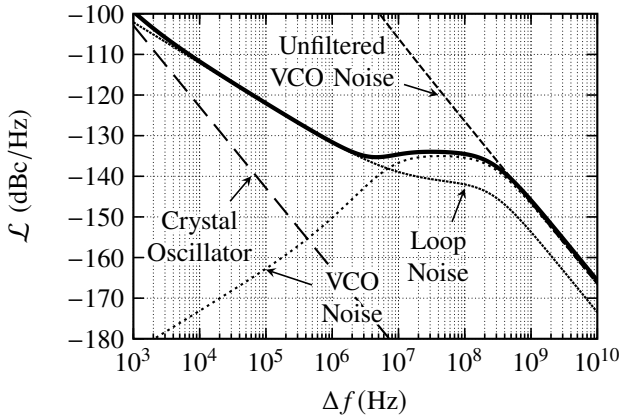

Fig. 9: Calculated/simulated phase noise spectrum of the entire SSPLL in lock (based on simulation data and models as well as measurement results of the LC oscillator)

TABLE I: Performance Comparison with State-of-the-Art Sub-Sampling Phase-Locked Loops

Work	**This Work**	JSSC'20 [9]	JSSC'15 [10]	ASSCC'19 [11]
Architecture	**SSPLL**	SSPLL	SSPLL + Div	SSPLL + Div
Oscillator Architecture	**High-Q LC**	LV-LC	SH QVCO	NMOS LC
Technology	**22 nm**	40 nm	40 nm	65 nm
Ref. Frequency (MHz)	**875**	200	40	50
Frequency Range (GHz)	**48 to 54**	12 to 16	53.3 to 63.3	55.5 to 62
PN @ 1 MHz (dBc/Hz)	**−132**	−115	−92	−95
Integrated Jitter[1] (fs)	**23**[2]	56[2]	200[2]	236[3]
Reference Spurs (dBc)	**−48**	−72	−40	−52
Power (mW)	**13**	7	42	23
Figure of Merit (dB)[4]	**−262**	−256	−208	−239

[1] $J_{\mathrm{RMS}} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2}\mathcal{L}(f)\,\mathrm{d}f}$ [12] [2] 1 kHz – 1 GHz [3] 1 kHz – 100 MHz

[4] $\mathrm{FoM} = 20\log_{10}(J_{\mathrm{RMS}}/1\,\mathrm{s}) + 10\log_{10}(P_{\mathrm{DC}}/1\,\mathrm{mW})$

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