A Charge Pump for Sub-Sampling Phase-Locked Loops with Virtual Reference Frequency Doubling

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***Abstract*—In this paper, a novel charge pump for sub-sampling phase-locked loops (SSPLLs) is presented. Contrary to the conventional charge pump, the proposed implementation eliminates the previously-required pulser. This is achieved by using all sample data from the ping-pong sub-sampling phase detector as opposed to only every second point, which enables the charge pump to run pseudo-continuous. This virtually raises the reference frequency by a factor of two, which is beneficial for the phase noise performance of the phase-locked loop while fulfilling the requirements for bandwidth of reference buffers, switches etc. Furthermore, eliminating the pulser enables a highly power-efficient charge pump design, leveraging higher SSPLL FoM. The proposed charge pump is implemented in a 22-nm fully-depleted silicon-on-insulator technology. The power and area consumption are reduced by roughly 80 % and 55 %, with similar effective gain, noise and offset performance to the conventional design.**

***Index Terms*—Sub-Sampling Phase-Locked Loop, SSPLL, Charge Pump, Sampling**

I. Introduction

In recent years local, regional as well as world-wide connectivity has continuously increased. Thus new wire-line and wire-less communication standards have emerged to satisfy ever-expanding requirements for data rates. To implement these new standards, high-performance transmitters and receivers for all kinds of communication technology are needed. These systems require periodic signals either as a clock for digital systems and analog-digital-conversion circuits or as radio-frequency (RF) signals for up/down conversion in mixers and local oscillators (LOs). With the increase of overall system complexity as well as the need for higher accuracy, bandwidth and data rates, the signal generators become more challenging to implement. More than power efficiency and circuit size, phase noise is the most dominating parameter of clock/signal generators. For this matter, sub-sampling phase-locked loops (SSPLLs) are the state-of-the-art architecture to implement low-phase-noise phase-locked loops (PLLs) [1]. This is due to the fact that sub-sampling phase detectors (SSPDs) inherently offer higher gain than conventional phase-frequency detectors (PFDs), hence leading to a suppressed loop noise.

A typical implementation of a sub-sampling phase-locked loop is shown in figure 1. The basic building blocks are the voltage-controlled oscillator, the loop filter (LF), the sub-sampling phase detector and the charge pump (CP) together with the pulser. The pulser turns the charge pump on only while the output signal of the phase detector is stable. The output current of the charge pump then takes the same form as the pulse, (dis-)charging the capacitors in the loop filter.

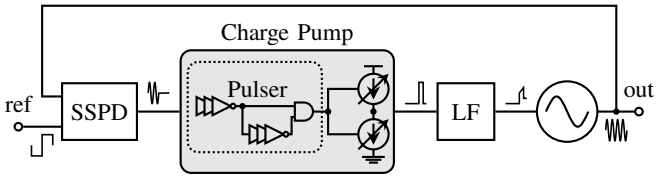

Fig. 1: Typical SSPLL system architecture with annotated associated signal waveforms and the implementation of the charge pump with a pulser (gray box)

Since the phase detector in an sub-sampling phase-locked loop is usually implemented as track-and-hold (T/H) circuit, the output signal exhibits a track- and a hold-phase. Since the charge pump should only operate on the signal in the hold-phase, it is turned on and off by an enable signal (a pulse). However, the generation of this by a so-called pulser is subject to significant process/voltage/temperature variations and consumes a considerable amount of power. Furthermore, for high-frequency millimeter-wave (mmw) SSPLLs, the sampling capacitor becomes very small (within a few femto farad). Here, early re-sampling of the track-and-hold signal avoids signal impairments or driving issues after the phase detector. Additionally, the remaining high-frequency signal parts are removed by re-sampling. In mmw-SSPLLs, differential ping-pong sampling is used to reduce the time-varying load of the oscillator [2]. In typical SSPLL implementations, one of the samplers only drives a dummy charge pump to equalize the sampler load, discarding every second sample [3], [4].

In this paper, a novel charge pump for sub-sampling phase-locked loops is presented. It leverages sampling done in a ping-pong fashion within the phase detector to run pseudo-continuously instead of pulsed. This paper is organized as follows: In section II the basic circuit implementation of the novel charge pump is shown, alongside a comparison with conventional implementations. Following that a circuit/noise analysis is given in section III, simulation results are given in section IV and section V concludes the paper.

II. Circuit Implementation

The charge pump in a sub-sampling phase-locked loop – as opposed to a regular PLL – is voltage-controlled, not pulse-width-controlled. Therefore, a CP for an SSPLL is implemented as a trans-conductance amplifier. Since this voltage is the output of a T/H, it has a track phase and a hold phase. During the

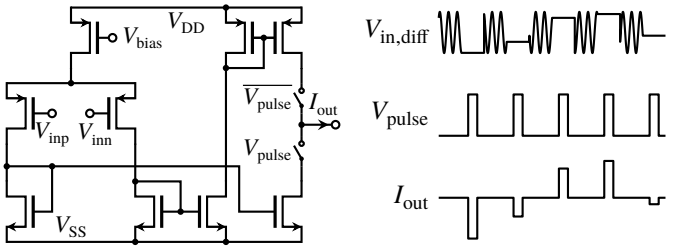

Fig. 2: Circuit implementation (left) and signals (right) of a conventional charge pump in a sub-sampling phase-locked loop

latter, the voltage is constant and the charge pump can be turned on by the pulse signal. An possible implementation of a conventional CP in an SSPLL is shown in figure 2, alongside with typical signals of the T/H signal and the enable pulse.

The proposed charge pump switches the voltage inputs, not the current at the output. The goal is to provide a stable current with only low-frequency contents to diode-connected transistors, which act as bias voltage generators for the output current mirror. The SSPLL reference signal (the clock) which controls the switches in the SSPD is used directly to enable/disable the input paths. This way, the summed currents at the nodes V_{left} and V_{right} never contain any high-frequency parts from the track phase of the output signal of the SSPD. Furthermore, this approach is also resistant against duty-cycle-variations, as those also affect the length of the two track phases.

Figure 3 shows the implementation of the proposed charge pump. In total, it features four inputs for the phase detector signal (two differential inputs with alternating track/hold phases) as well as two pins for a differential clock input signal. One bias current feeds two differential pairs. In each differential pair, only one branch is turned on at all times. Even with the respective switch turned off, each branch injects unwanted current with high-frequency contents in the diode-connected transistors. In high-frequency SSPLLs, this can lead to serious disturbances on the bias voltage of the diode-connected transistors. To counteract this, always-off dummy paths with the opposite signal are added. Ideally, these currents cancel out perfectly. In reality, non-linearity and mismatch leads to non-perfect cancelling, however, even in this case this technique is very effective. The only drawback of this approach is a slightly increased load capacitance for both the phase detector signal and the clock. However, the additional capacitance is still insignificant compared to the lumped sampling capacitance of the phase detector. The higher load also does not affect the reference signal as its frequency is much lower.

In a classical SSPLL implementation, every second sample from the SSPD is discarded. In the proposed charge pump, both hold phases from the alternating phase detector are used. This raises the reference frequency virtually by a factor of two. A higher reference frequency is beneficial for PLL output phase noise [5], reference spurs [6], capture range [7] and avoidance of false locking [8], [9]. Therefore, the virtual rise of the reference frequency is a significant advantage with this charge pump design. Furthermore, the actual reference frequency does not change which means that there are no further constraints on the circuit implementations such as the track-and-hold switches or the charge pump. It is only that the SSPLL with the novel charge pump uses all available sample data, whereas the conventional implementation discards every second sample. This inhibits the SSPLL to lock to odd multiples of the reference frequency.

The proposed charge pump implementation does not depend on a pulser to enable/disable the output current. This has two advantages: The power consumption of a pulse-generating circuit is not insignificant and typical implementations only support a narrow range of reference frequencies [10], [11], since it must be ensured that no overlap between the reference signal and the pulse occurs. In the proposed design, these issues are simply not present. This enables further improvements in low-power high-performance mmw-SSPLLs as well enabling SSPLLs with arbitrary reference frequencies. This is especially interesting for two-stage SSPLLs.

Precise control of the loop dynamics of the PLL enables lowest noise and optimal stability margins. Therefore, precise control of the effective charge pump gain is also required. In charge pump implementations with a pulser, the pulse width can be used to control the gain of the charge pump. In the proposed implementation, the gain of the charge pump can easily be controlled by the ratio of the number of fingers in the output path. Since the involved signals are of lower frequency, simple on/off switching of the transistors is possible. The effective gain of a pulse-controlled charge pump can be expressed as

$$G_{\text{m,CP,eff}} = G_{\text{m}} \cdot V_{\text{sample}} \cdot T_{\text{pulse}} \cdot f_{\text{ref}} \tag{1}$$

where G_{m} is the overall trans-conductance of the charge pump, V_{sample} the sampled oscillator voltage in the hold phase, T_{pulse} the pulse width of the enable signal and f_{ref} the reference frequency. By changing T_{pulse}, the effective charge pump gain can be adjusted. For the proposed charge pump, the gain expression is similar, only that $T_{\text{pulse}} \cdot f_{\text{ref}} = 1$. This means that the charge pump gain has to be adjusted with G_{m}, which is readily available by changing the trans-conductance of the output devices. The overall trans-conductance G_{m} depends on the input devices and the output current mirror:

$$G_{\text{m}} = 2 \cdot g_{\text{m,input}} \,/\, g_{\text{m,diode}} \cdot g_{\text{m,out}} \tag{2}$$

Besides high-frequency signal injection, clock overlap also poses a design challenge. While this charge pump is immune to changes in the duty cycle, overlap between the positive and the negative clock input lead to direct appliance of the input signal in its track-phase. Appropriate clock buffering is used to mitigate these effects, where a high crossing point of the clock signals is chosen. This way, at maximum only one pMOS switch is turned on at all times. For the physical implementation the path lengths of all clock inputs must be matched. Clock crossing issued in the proposed design where checked with random variations of the devices (monte-carlo-simulation). The variation shows no potential problems.

As seen in figure 3, the proposed design uses two separate supply voltages. This is because the input voltage range of the

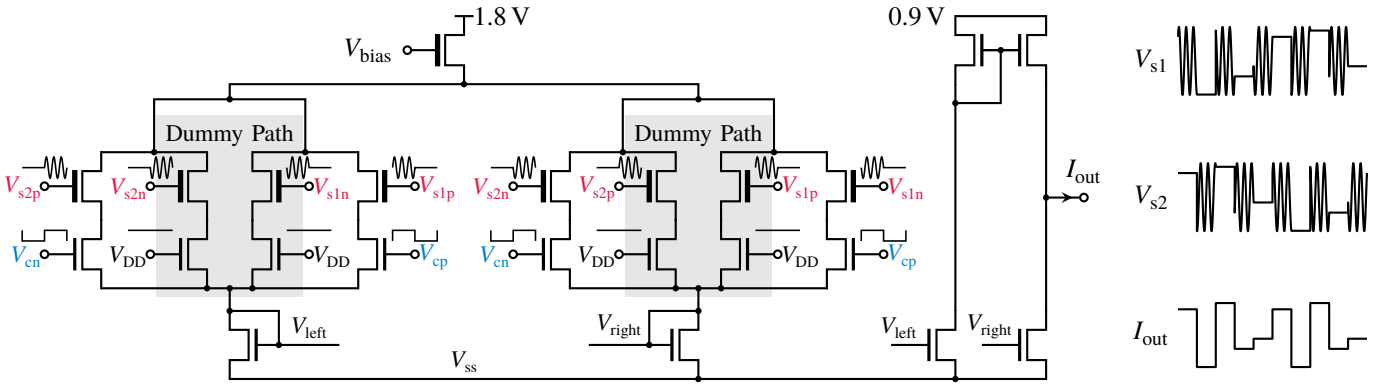

Fig. 3: Top-level circuit implementation of the novel SSPLL charge pump (left) and corresponding timing diagram (right)

differential pair needs to be extended to match the voltage swing of the oscillator output. However, this is not intrinsic to this design, so a single-power-supply design is also possible. The input path creates the bias voltages for the output current mirror, which can be held very simple (as in this implementation). In the conventional implementation of the charge of an SSPLL the output path contains switches which reduce the available head room for the current source as well as introduce (usually negligible) charge injection on the output node. In the proposed implementation the re-sampling is provided by the input stage, eliminating any switches in the output path.

III. Noise Analysis

The loop noise of an SSPLL is greatly suppressed due to the high detector gain. However, for medium-to-low offset frequencies, the loop noise is a significant contributor to the overall integrated phase noise of the PLL. This originates mostly in the charge pump [5], so it is crucial to find the devices with the largest contribution. In both the conventional and the proposed charge pump design, the main devices for noise considerations are the input transistors of the differential pair as well as the transistors of the output current mirrors. The input devices of the differential pair add noise proportional to their trans-conductance. The output-referred current noise expression for both charge pump architectures will be shown next. For this, it will be assumed that all relevant current paths are turned on and that the switches do not contribute to the total noise. The noise current depends on the trans-conductances $g_{m,outn}$ and $g_{m,outp}$ of the output current devices (nMOS and pMOS). The noise of the input stage is represented as a voltage at the gates of the nMOS current devices by $\overline{V_{left}^2}/\Delta f$ and $\overline{V_{right}^2}/\Delta f$. The output-referred current noise amounts to

$$\frac{\overline{i_{out}^2}}{\Delta f} = 4k_B T(g_{m,outn} + g_{m,outp}) + g_{m,outn}^2 \frac{\overline{V_{left}^2}}{\Delta f} + g_{m,outp}^2 \frac{\overline{V_{right}^2}}{\Delta f} \quad (3)$$

It is assumed that the input front-end contributes the same noise for both architectures. This is reasonable, as equal-sized devices and bias currents are used for both charge pumps. Then, in order to minimize the output-referred current noise, the trans-conductances $g_{m,outn}$ and $g_{m,outp}$ should be small. Since the overall charge pump trans-conductance is scaled by $T_{pulse} \cdot f_{ref}$, $g_{m,outn}$ and $g_{m,outp}$ can be even smaller for the proposed charge pump. Effectively, this equalizes the gain and noise of both architectures. While the proposed charge pump exhibits lower noise, it also runs continuously. Since the conventional charge pump is not turned on at all times, its effective noise injection is lower, scaled by the duty cycle. The possible gain reduction and the higher duty cycle cancel out, leading to no or only insignificant changes for the overall noise performance.

IV. Simulation Results

The proposed charge pump was implemented in a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology. The circuit is built for an SSPLL with an output frequency of 56 GHz and a reference frequency of 875 MHz, corresponding to a multiplication factor of 64. The charge pump was simulated stand-alone as well as embodied in a closed-loop ideal SSPLL to show the features and advantages. For comparison purposes, a second, conventional charge pump was implemented in the same technology in order to match the overall circuit behavior as closely as possible. As the main parameter of the charge pump used in an SSPLL is the current gain, both circuits where built to realize equal trans-conductances.

Figure 4 shows the simulated effective gain of the conventional and the proposed charge pump under the influence of process and temperature variations. The target trans-conductance is 400 µS. The effective gain variation for zero-volt inputs is very similar for both charge pump architectures. The proposed implementation shows a broader transfer characteristic, this is however not important as the negative feedback of the SSPLL will lock at the point of maximum gain anyway.

Figure 5 shows the simulated supply current of the conventional and the proposed charge pump. For the same effective gain, the proposed charge pump draws a significantly reduced current. Furthermore, while both circuits exhibit similar disturbances due to the clock, the conventional implementation additionally generates a lot of noise due to the inverter chain in the pulser. The root-mean-square (RMS) supply current consumption is reduced by almost 80 %, from 1.756 mA to 374 µA. This is mainly due to the elimination of the

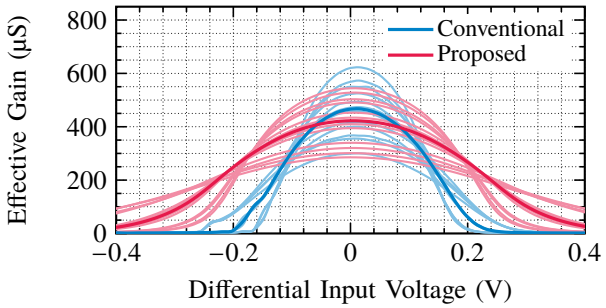

Fig. 4: Simulated effective charge pump gain against input voltage with inclusion of process and temperature variations. The typical corner is emphasized

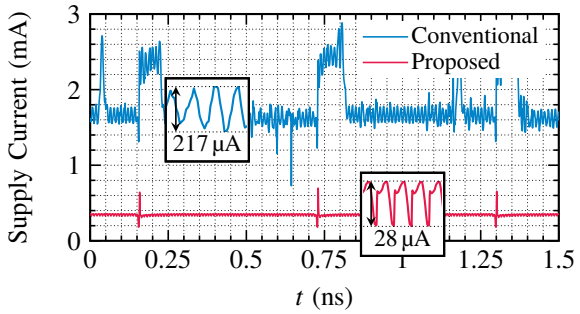

Fig. 5: Simulated supply current consumption of the conventional and the proposed SSPLL charge pump

pulse generator. The implementation with inverter chains (see figure 1) draws significant supply current and introduces a much bigger supply current ripple than the rest of the circuit.

Figure 6 shows the simulated output current noise of both charge pump architectures for an equal effective gain. As predicted in section III, the effective output noise is equal.

Table I shows the comparison of the performance metrics between the conventional and the proposed implementation of the charge pump for a sub-sampling phase-locked loop. All parameters except the input offset voltage show an improvement, most notably the RMS supply current with almost 80 % and the area with roughly 55 %. The input offset voltage of the proposed design is slightly increased by 35 %. In an sub-sampling phase-locked loop however, the input offset voltage of the charge pump is not of a larger concern, as the negative feedback of the entire PLL cancels the offset. It merely relates to a slight static phase shift between the reference and the output signal.

The area comparison only entails the channel area of the transistors of both circuits. For this discussion it is assumed that the overhead for routing, guard rings, power grids etc. scales approximately linear with the active area. Furthermore, for the conventional charge pump, due to the switching action, a dummy path is added which is turned on when the main path is off. This is in order to ensure proper operating conditions for the current sources so that they do not turn off. In turn, some sort of replica action or stabilization is required, which can be done by adding a copy of the SSPLL filter capacitor to the

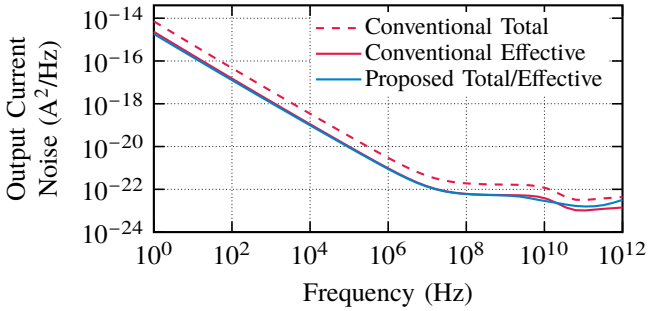

Fig. 6: Simulated total/effective output current noise of the conventional and the proposed SSPLL charge pump

TABLE I: Comparison between simulated results of the conventional and the proposed SSPLL charge pump implementation

Parameter	Unit	Conventional	Proposed	Change (%)
RMS Supply Current	mA	1.756	0.374	**−78.7**
Gain Variation	%	70	64	**−8.6**
Input Offset Voltage (σ)	mV	11.24	15.2	+35.7
Supply Current Ripple	µA	217.2	28.6	**−86.8**
Active Transistor Area	µm^2	12.48	5.39	**−56.8**

dummy path or by stabilizing with an operational amplifier ([1], [6], [12]. Both techniques have quite a serious area penalty, which is not included in table I. The proposed charge pump is operating continuously and never turned off. Therefore, such stabilizing methods are not required, rendering this design even more area efficient than shown.

V. Conclusion

In this paper, a novel charge pump for sub-sampling phase-locked loops was presented. The charge pump does not rely on a clock pulser to generate the enable signal, which significantly reduces the power consumption and the supply voltage disturbances of the entire circuit. The novel implementation shows no noise penalty, as the voltage-to-current characteristic and the corresponding transistors can be biased in the same manner. As a second significant change the charge pump enables a virtual doubling of the reference frequency, as the output signals of both track-and-hold circuits of the SSPD are used to control the charge pump.

The proposed charge pump provides a higher effective gain with less variation across process and temperature while significantly reducing the power and area consumption of the circuit. It is applicable to any sub-sampling phase-locked loop architecture with the sub-sampling phase detector operating in a ping-pong fashion. A silicon verification in a 56-GHz-SSPLL is planned and being worked on.

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