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A 56 GHz 19 fs RMS-Jitter Sub-Sampling Phase-Locked Loop for 112 Gbit/s Transceivers

P. Kurth, K. Misselwitz, U. Hecht, F. Gerfers

Technische Universität Berlin

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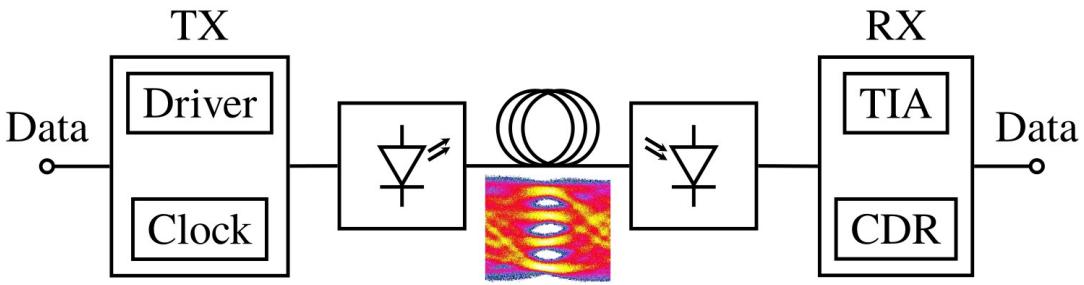
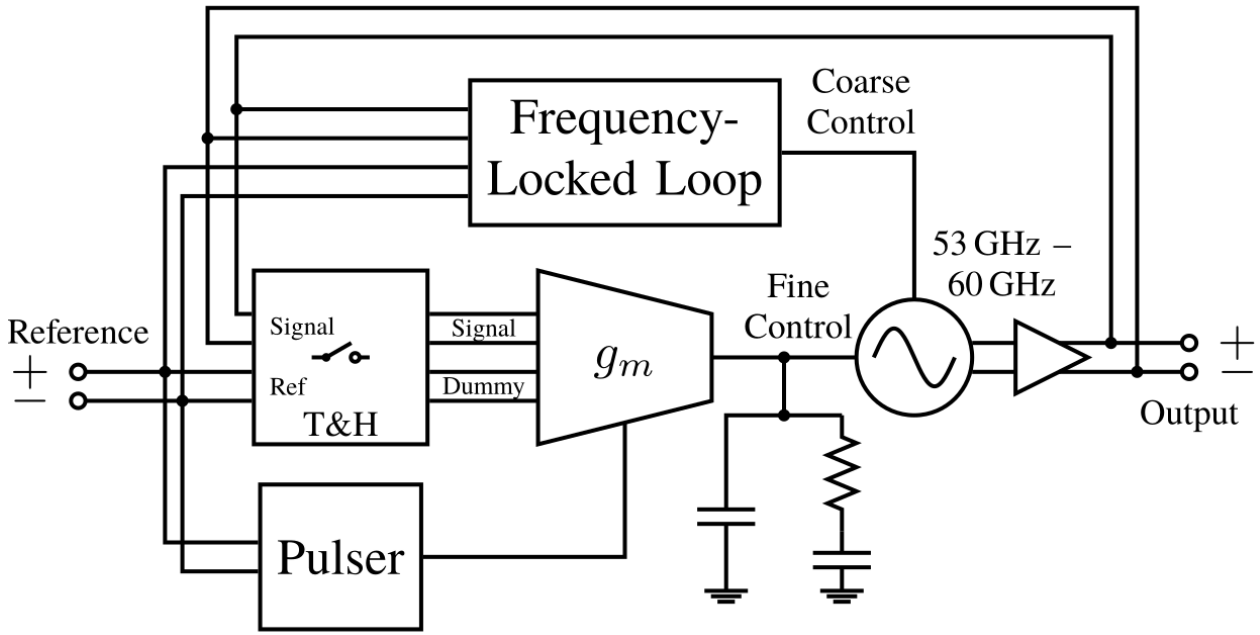
Motivation and System Overview

- Next-generation optical wire-line with 400 Gbit/s, 100 Gbit/s per lane
- 4-Level Pulse-Amplitude-Modulation with full-rate 56 GHz clock frequency
- Low cost vertical-cavity surface-emitting laser (VCSEL) diode at the transmitter site
- Silicon photonics PIN diode at the receiver site
- Single-chip solution

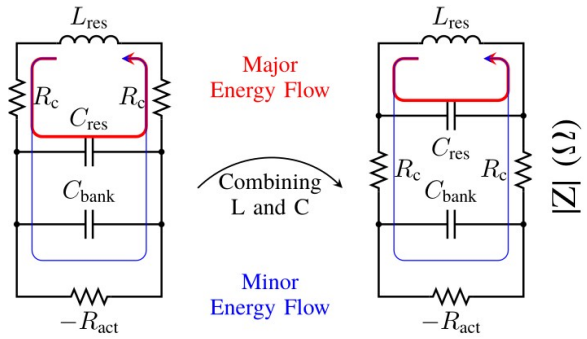


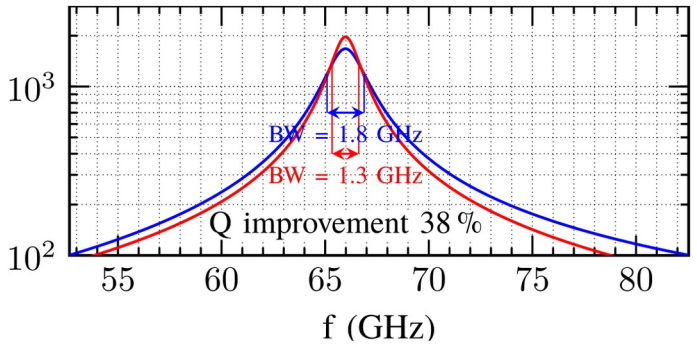
- Sub-Sampling Phase-Locked Loop for phase lock with 1 GHz reference
- PFD-based type-II PLL for frequency lock
- Fundamental 56 GHz LC-VCO with buffer
- Differential track-and-hold
- Two-voltage-domain charge pump

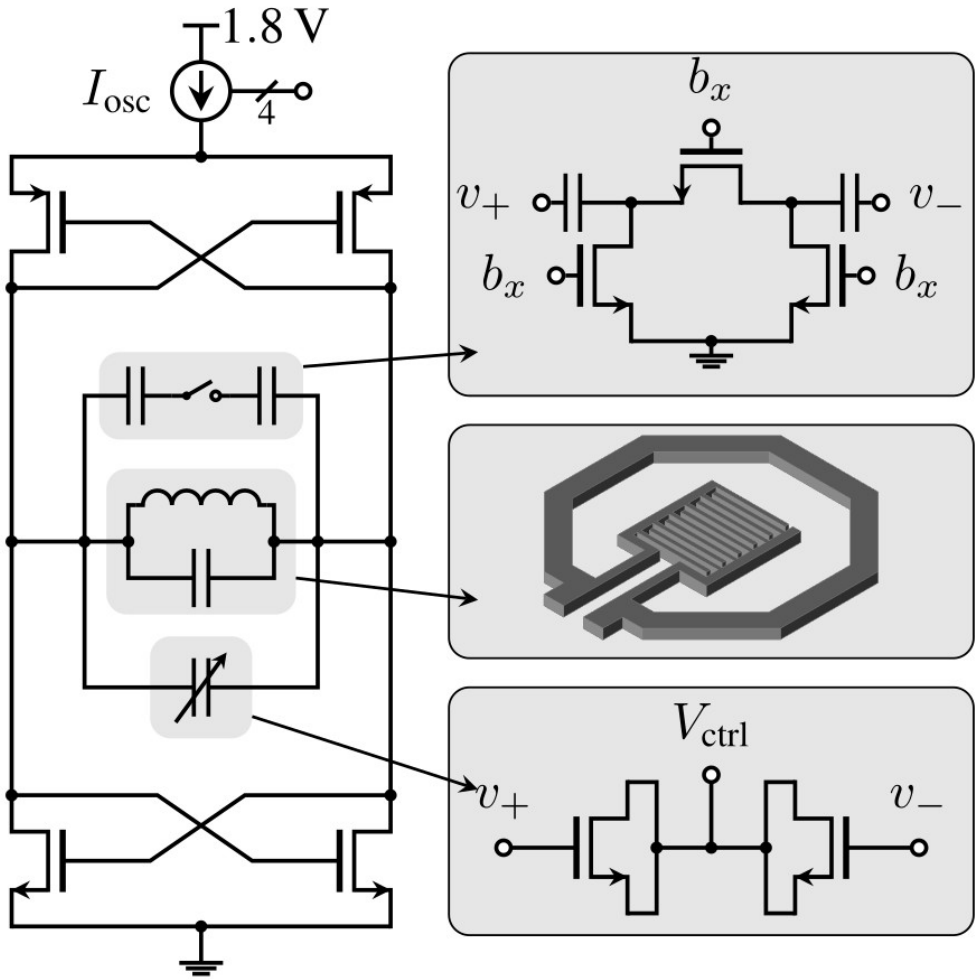


VCO Implementation

- Fundamental Cross-Coupled LC-Oscillator
- Specialized combined LC-Resonator
  - Ultra-compact
  - High-Q
  - Increases Q by 38 % compared to separated implementation
- Switched capacitor bank for coarse tuning
- nMOS-varactor for fine tuning

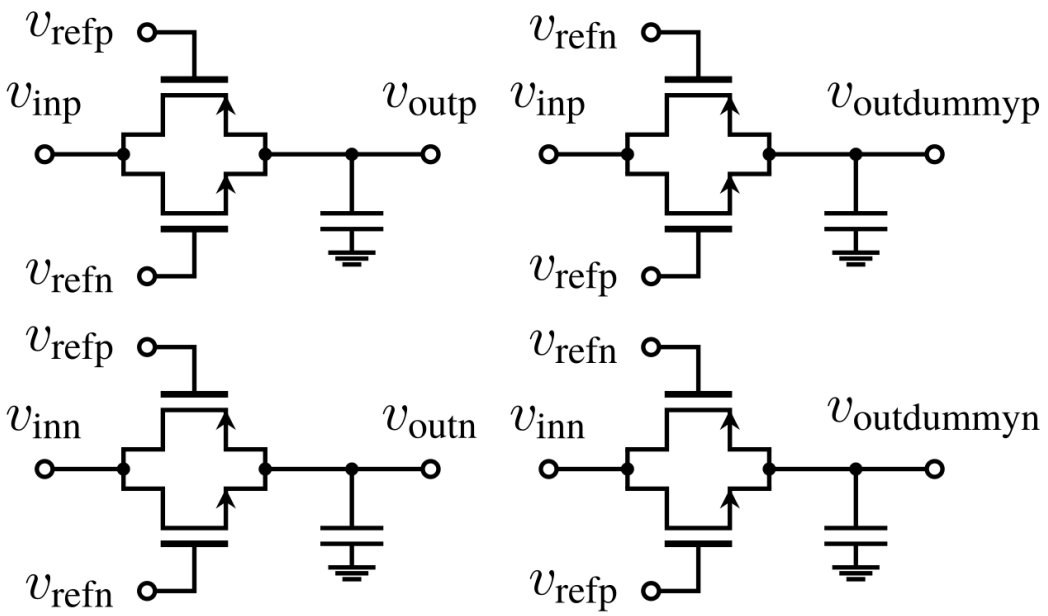




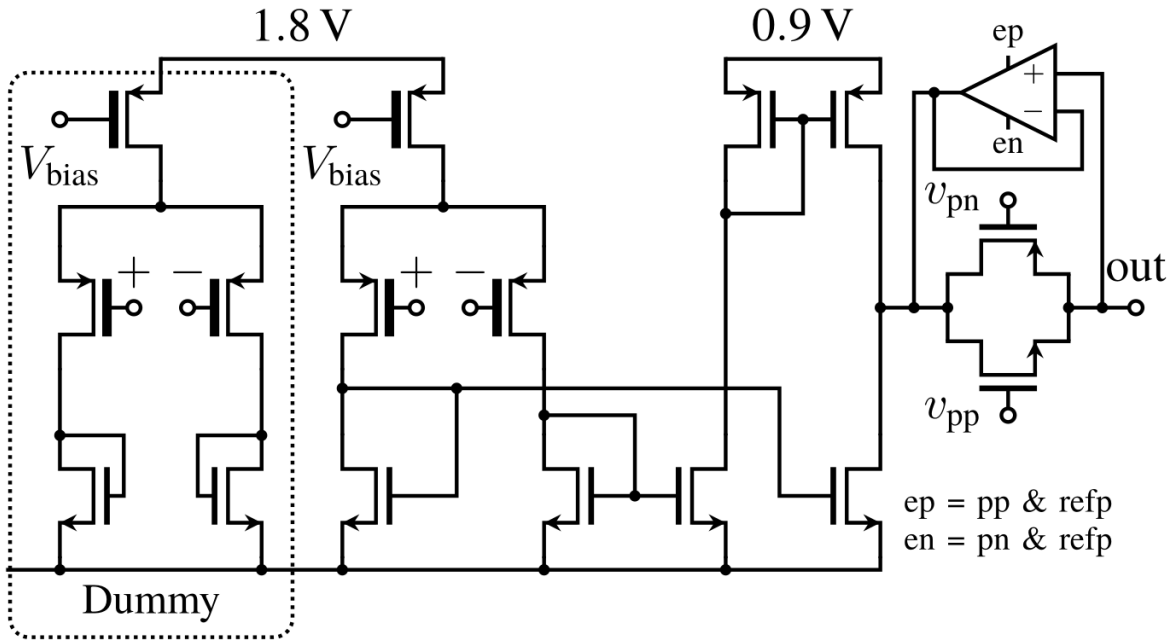


Track-and-Hold and Charge Pump

- Two track-and-hold (T&H) circuits in ping pong fashion to reduce reference spur
- Simple transmission gates sufficient
- Slight bandwidth limitations, but high enough for proper PLL operation

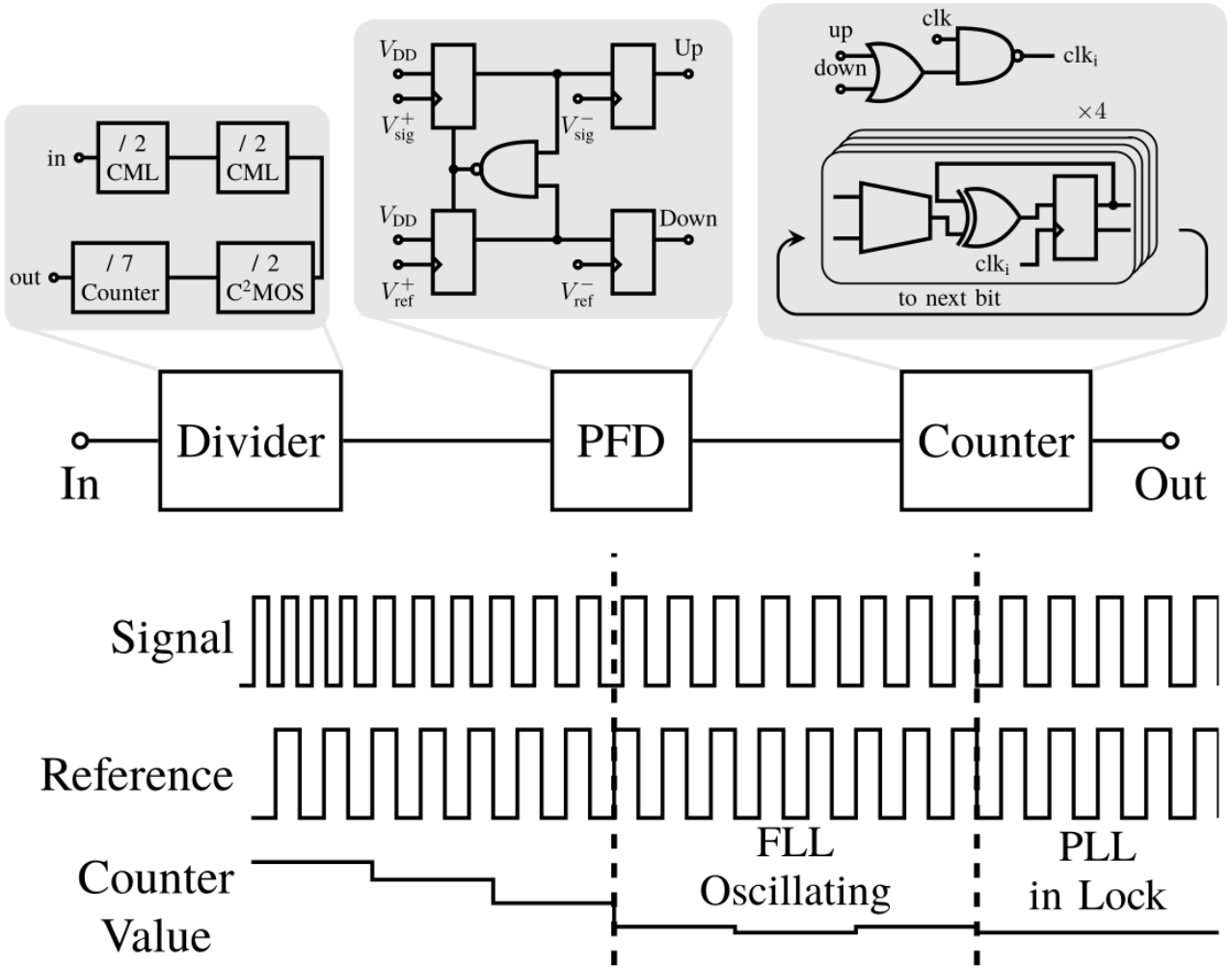


- pMOS-input OTA
- Two voltage domains: 1.8 V and 0.9 V
- Input pair operating range covers all sample voltages
- Output branch with core devices for shorter length/higher speed



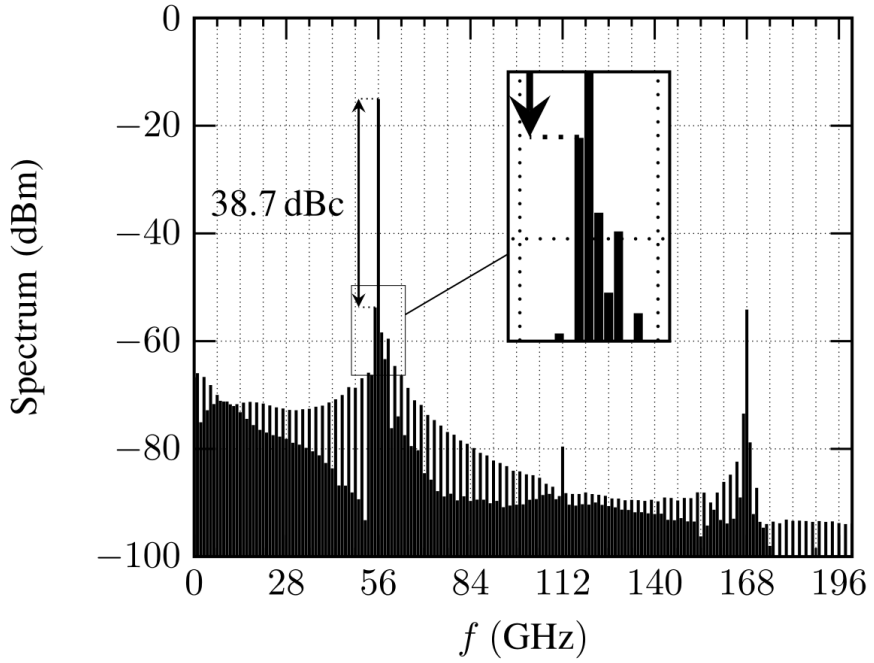
Frequency Control

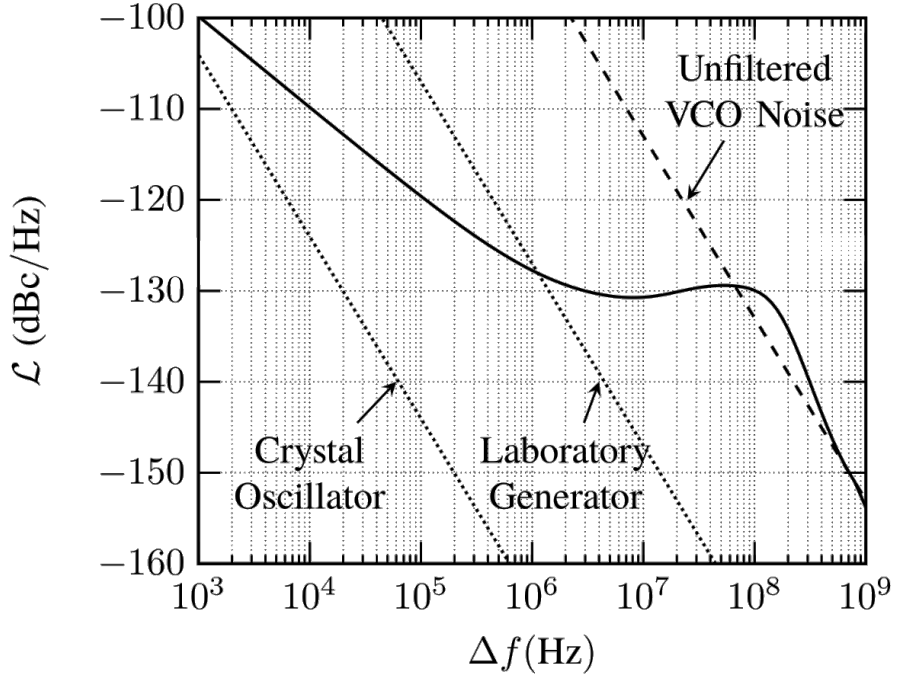
- Secondary Loop directly controlling coarse oscillator tuning
- Semi-digital approach: PFD and counter synthesizable
- Phase-Frequency Detector with dead-zone
- Divider: 2 x 2 x 2 x 7 = 56
  - 2 x CML with intermediate buffer
  - 1 x TSPC
  - 1 x C²MOS counter
- Up/Down Counter to track and set appropriate PLL frequency



Simulation Results

- Implemented in 22 nm FDSOI
- Simulation across process corners and mismatch simulations
- Layout-extracted schematics (VCO) together with pre-layout schematic
- with estimated parasitics
- Worst-case reference spur: -38.7 dBc
- Integrated RMS-jitter (1 kHz – 1 GHz): 19 fs, power consumption: 32 mW → FoM: -259 dB





Thank you for your attention!