A 56 GHz 19 fs RMS-Jitter Sub-Sampling Phase-Locked Loop for 112 Gbit/s Transceivers

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***Abstract*—This paper presents a 56 GHz Sub-Sampling Phase-Locked Loop (SSPLL) for an optical transceiver system. It employs an LC oscillator without frequency multiplier featuring a novel combined resonator for high purity signals, a differential track-and-hold with dummy samplers, a charge pump with feedback amplifiers and specialized input pairs for high voltage operation. The sub-sampling architecture allows for ultra-low phase noise at low offset frequencies, while far-out phase noise is minimized due to the used high-purity oscillator. The phase noise at an 1 MHz amounts to −127 dBc/Hz, resulting in a total integrated jitter of 19 fs (range from 1 kHz to 1 GHz). This 56 GHz SSPLL enables next-generation wire-line optical communication standards with over 100 Gbit/s.**

***Index Terms*—Sub-Sampling Phase-Locked Loop, Frequency Synthesizer, Millimeter-Wave, LC Oscillator, Wire-line, Optical Transceiver**

I. Introduction

Next-generation optical wire-line communication standards aim for 400 Gbit/s in four lanes, which requires at least 100 Gbit/s per lane. A good compromise between modulation depth and speed is sending two symbols per period (pulse-amplitude modulation 4; PAM-4) with a clock frequency of 56 GHz, leaving room for error correction and overhead. This enables the use of vertical-cavity surface-emitting lasers (VCSEL) with typical bandwidths of around 30 GHz [1]. These devices allow (with multi-mode fibers) for cheap assembly at the cost poor performance, as these components exhibit significant imperfections such as non-linearities and stimulus-dependent relaxation oscillations. This requires either non-linear equalization filters [2] or linear versions with many taps [3], including sub-unit-interval (UI) taps. For this, high precision frequency synthesizers with ultra-low phase noise/jitter are needed.

Figure 1 shows the overall system architecture of an optical transceiver. The transmitter (TX) and receiver (RX) chip are to be realized as single-chip solution in CMOS with the driver, the slicer, clock-and-data recovery (CDR) and the clock generation on each chip. The tolerable root-mean-squared (RMS) jitter of the clocking system amounts to less than 75 fs for a transceiver system with two bits for symbols and four bits for equalization and a target bit-error-rate (BER) of 10^{-12} [4].

Modern high-performance phase-locked loop (PLL) designs can be either analog or digital, where all-digital PLLs have been starting to meet/exceed analog PLL performance [5]. Among analog PLLs, the major implementation techniques include injection-locked PLLs [6] and type-II PLLs with a phase-frequency detector (PFD). Another type of phase detector can be built by using a track-and-hold (T&H) in a so-called sub-sampling PLL (SSPLL). This type has been proven to enable lowest-noise PLLs while also having low power consumption [7]. The main advantage of SSPLLs is their lack of a frequency divider, which increases the effective charge pump gain and therefore lowers the loop noise by N^2, where N is the ratio of the output and reference frequency [7].

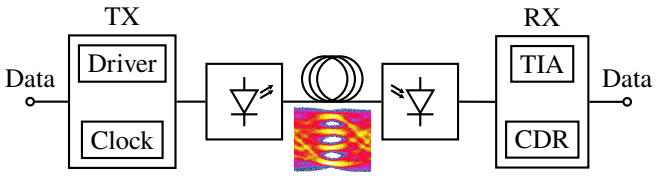

Fig. 1: Top-level system architecture of the optical wire-line transceiver, including transmitter (TX), receiver (RX), laser (VCSEL) and photo diode.

This work presents the design of a sub-sampling phase-locked loop to be used as frequency synthesizer in a complete optical transceiver system. The paper is organized as follows: The overall system architecture is discussed in section II, where the individual components and their features are highlighted. The simulation results are shown in section III and section IV concludes the paper.

II. Implementation

Figure 2 shows the top-level architecture of the entire PLL. The output of the oscillator is buffered by an intermediate buffer and then sampled by the track-and-hold. The charge pump following the T&H only operates during the hold phase, enabled by a pulse signal (generated by a dedicated pulser). The loop filter is a simple low-pass with two poles and one zero. Besides the sub-sampling loop, a classical type-II PLL with a phase-frequency detector is used for frequency locking, as the sub-sampling loop can lock to any integer multiple of the reference frequency.

The PLL is designed for an input reference frequency of 1 GHz and an output frequency of 56 GHz. It is an integer-N architecture, as no fractional tuning is needed for the application. As the out-of-band phase noise is dominated by the voltage-controlled oscillator (VCO), an LC-oscillator is used since these provide highest phase noise performance of integrated

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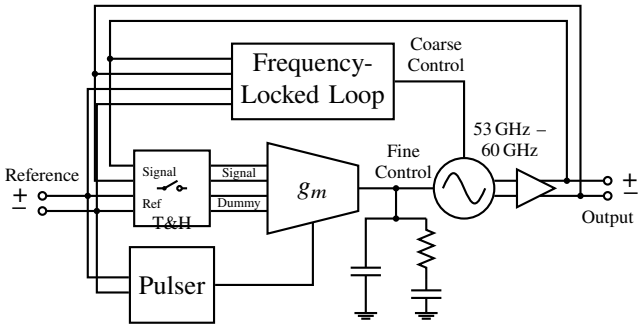

Fig. 2: Top-level architecture with both the sub-sampling and the frequency-locking loop.

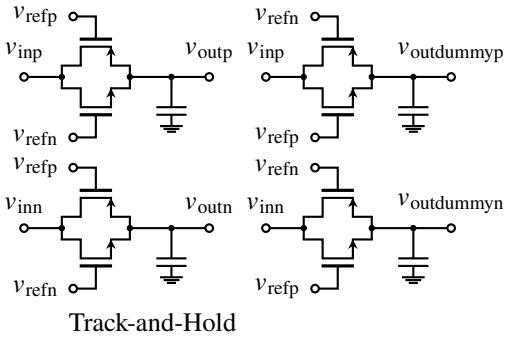

Fig. 3: Implementation of the track-and-hold (dummies not shown) and the intermediate oscillator buffer with AC coupling.

oscillators. As the in-band phase noise of an SSPLL is very low, the loop bandwidth is maximized to filter out most of the oscillator noise. The poles and zeros of the filter are then accordingly chosen while maintaining system stability. Following this overview, the critical building blocks will be highlighted in more detail.

A. Phase detector: Track-and-hold

The track-and-hold faces the highest frequencies in the loop, as it samples the oscillator directly, without any intermediate frequency dividers. This means that the sampling capacitors need to be very small as a bandwidth of more than 56 GHz is needed for appropriate settling. The sizing of the switches is a compromise between the on-resistance and the parasitic capacitances. Furthermore, the oscillator output signals cover the entire supply range, requiring transmission gates as switches, as opposed to simple nMOS/pMOS switches. To reduce uneven oscillator loading, the T&H operates in a ping-pong fashion and therefore uses four transmission gates in total (two for differential operation in each ping-pong phase). The sampling capacitors are as low as 5 fF, but as the loop noise is strongly suppressed by the high phase detector gain this does not impair the overall noise performance of the PLL [7].

The sampler poses a heavy load for the oscillator, therefore an intermediate oscillator buffer is implemented. It is built as simple nMOS inverter with pMOS current source load. The oscillator output signal is AC coupled into the buffer. The buffer is also needed for isolating the oscillator from the trackand-hold, as a direct connection increases reference spurs by loading the oscillator.

B. Charge Pump

The charge pump converts the sampled oscillator output voltage into a proportional current. The used transistors have a variety of oxide thickness for different voltages: The front-end differential pair uses transistors with medium thickness as to enable operation over the entire voltage range of the oscillator signal. As this requires rail-to-rail action, a differential pair with pMOS input and a supply voltage of 1.8 V is used, allowing input signals up to the core voltage of 0.9 V. The current mirror for the differential pair is therefore built with high-voltage transistors, as speed is not important for these devices. The

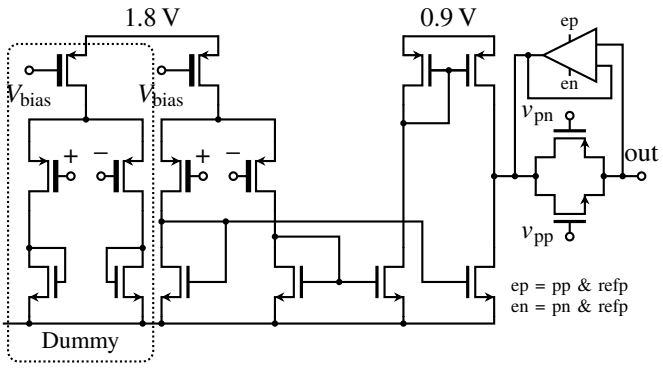

Fig. 4: Charge pump with dummy differential pair, feedback amplifier and split power supplies. The input transistor are thick-oxide devices.

back-end of the charge pump is then built with core devices, as they enable fast switching. Besides the input differential pair, the charge pump features a second, identical differential pair which follows the dummy sampler in order to equalize the loading. This significantly reduces the reference spurs. The mirrored current of the differential pair is only passed to the output at a reduced pulse duration, which is generated by the pulser. This circuit uses delay- and AND-gates for generating appropriate pulse signals. The charge pump uses a feedback amplifier for to stabilize the circuit operating point during the transitions. A further improvement could be a auto-zeroing action which lowers flicker noise input offset voltage [8], but the amount of phase noise in the respective frequency range has only little impact on the overall integrated jitter, as shown in the simulation results. The input offset voltage of the charge pump introduces no performance issues, as this only translates into a locking point where a point different from the zero crossing of the oscillator signal is sampled, resulting only in a negligible constant phase shift.

C. LC-Oscillator

The LC-oscillator uses a standard architecture for simplicity with two complementary cross-coupled pairs, but optimizes the quality of the resonator by integrating both the inductor and the capacitor in the thick, high-quality RF-capable metal usually

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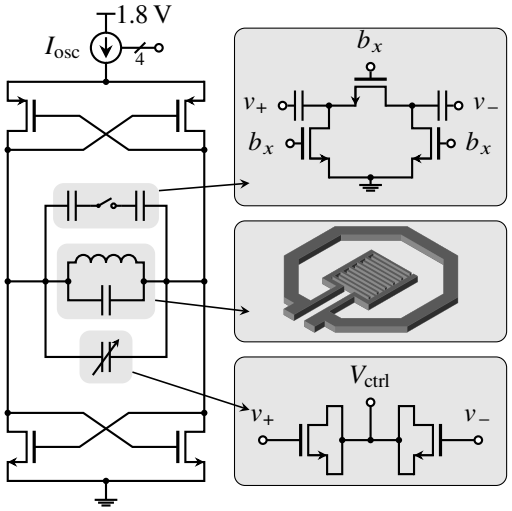

Fig. 5: Core LC-voltage-controlled-oscillator with combined resonator on RF metal. The bias current and the capacitive bank both have four bits for calibration.

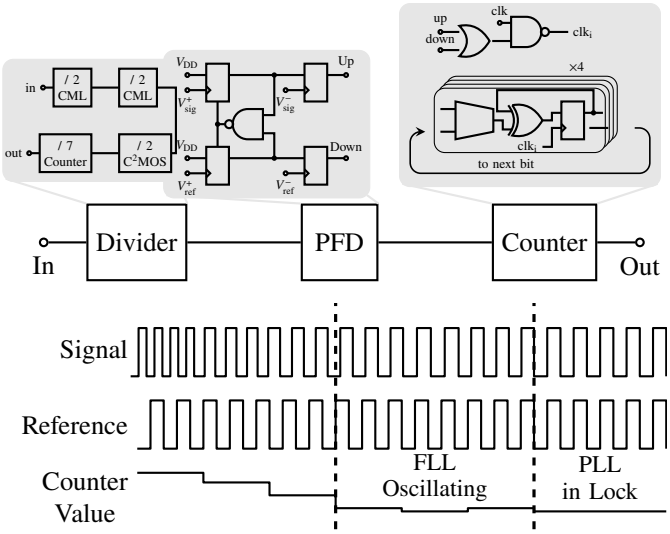

Fig. 6: Implementation of the frequency-locked loop control with corresponding waveforms. The PLL core ensures correct locking when the frequency is in range.

used for inductors. This removes the harmful interconnect resistance between the two elements which greatly influences the quality factor of the entire resonator. As this governs the overall purity [9], the noise performance of the oscillator is optimized in this way. Furthermore, this results in a very area-efficient design.

The analog tuning is done with MOS varactors, the coarse frequency can be calibrated with a capacitive bank with four binary-weighted bits. The oscillator can furthermore be tuned in its biasing via the top current source, which also uses four bits for calibration. The simulated phase noise of the oscillator at an offset frequency of 1 MHz is −95 dBc/Hz with a flicker noise corner in the same frequency range. However, the loop bandwidth of the PLL is high enough to filter out any flicker phase noise of the oscillator. The analog tuning range of the oscillator is large enough to cover the possible locking points of the SSPLL (steps of 1 GHz). The capacitive bank has a doubled resolution (approximately 500 MHz) to ensure coverage of the entire tuning range over all possible process variations. The entire tuning range is around 7 GHz, from 53 GHz to 60 GHz. The oscillator consumes 4.5 mW from a 1.8 V power supply and achieves $\mathcal{L} = -93$ dBc/Hz at 1 MHz, resulting in a FoM of −181.4 dBc/Hz.

D. Frequency Lock

The nature of the sub-sampling phase detector leads to the PLL not having an absolute frequency reference, therefore a locking to any integer multiple of the reference frequency is possible. To solve this issue, a frequency-locking mechanism is needed, which can be done by incorporating a typical type-II PLL next to the SSPLL. Here frequency dividers are needed, as a regular phase-frequency detector (PFD) is used to compare the reference and output frequency. The PFD implementation adds a deliberate dead zone, as only frequency lock (no phase lock) is needed. The output frequency needs to be divided by 56, which can be broken into $2 \times 2 \times 2 \times 7$. The first two by-two-dividers are built in current-mode-logic (CML) as these dividers face highest signal frequencies of 56 GHz and 28 GHz. A resistive-loaded differential pair with nMOS-input acts as buffer between both CML stages. The third stage is implemented with two clocked CMOS (C^2MOS) logic, as this enables medium-to-high speeds at low power consumption. For the last divider stage, a typical latch-based divider with NOR-gates is implemented [10] with the C^2MOS latches as D-flip-flops. The final block in the frequency-locked loop is a digital counter with an up- and down-input. As long as the reference and the divided output frequencies do not match, the counter will either receive more ups or downs. Only in approximate lock the counts will be the same. The counter has four bits, all of which are used to control the four bit binary-weighted capacitive bank of the LC-oscillator.

Figure 6 shows the implementation of the frequency-locking loop with its individual circuits and waveforms. As the frequency can only be controlled coarsely, the counter value will jump between two values, while the PLL core is still locking. Once the entire PLL is in lock, the PFD will not detect any frequency deviation and the counter value will stay constant. In this state, the entire frequency-locking system can be turned off, as the core PLL will not loose phase lock, therefore always keeping the right ratio between the input and the output frequencies. This significantly increases the efficiency of the entire PLL, as the CML frequency dividers consume a lot of power.

III. Simulation Results

The SSPLL is built in a 22 nm FDSOI CMOS technology. It is simulated in periodic steady state (PSS) simulation mode in various process corners and with monte carlo random sampling.

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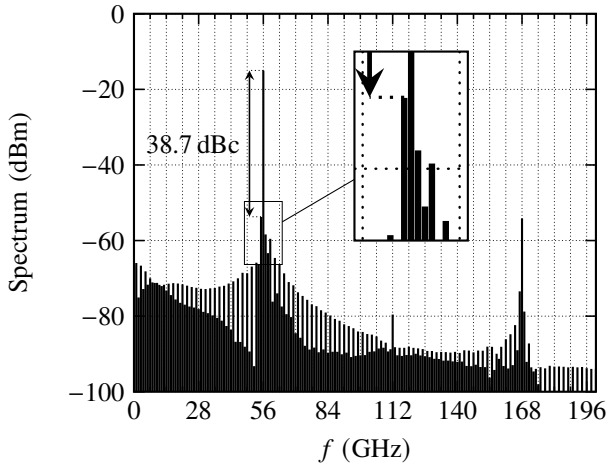

Fig. 7: Simulated spectrum of the entire SSPLL in lock; The spacing of the points is the reference frequency (1 GHz).

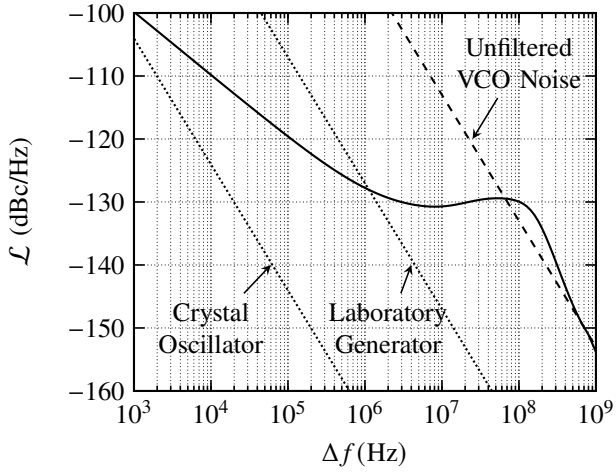

Fig. 8: Simulated phase noise profile of the entire SSPLL in lock with annotated VCO noise and possible reference phase noise profiles. The loop bandwidth is around 100 MHz, the integrated RMS jitter from 10 kHz to 1 GHz amounts to 18.5 fs.

Pre-layout parasitic estimations have been included. For some circuits such as the oscillator more realistic parasitic models have been extracted as these layouts have been already created.

Figure 7 shows the simulated spectrum of the SSPLL. The circuit shows only low power reference spurs (−38.7 dBc) and some harmonics. The latter however pose no issue as the third harmonic is so high in frequency that it is being filtered out. The second harmonic is unwanted in communication systems running at 112 Gbit/s, but the power is so low that this is unproblematic. Simulations with circuit mismatches included show no further raise of the second harmonic.

Figure 8 shows the phase noise of the PLL. The bandwidth is around 100 MHz, an optimal partition between loop noise and VCO noise. The lower frequency range is dominated by the flicker noise of the charge pump. Here a chopped amplifier approach could be used in order to lower the noise in this frequency band, however for some reference generators this is negligible, as the phase noise of the reference signal will dominate. The graph includes the phase noise profiles of a commercial high performance laboratory signal generator [11] as well as a highest purity crystal oscillator module [12]. The former totally shadows the flicker noise. Furthermore, the influence of this region on the total jitter is not high (approximately 2 %). The total integrated jitter from 1 kHz to 1 GHz amounts to approximately 18.5 fs.

TABLE I: Performance Comparison

Work	**This Work**	JSSC'20 [14]	JSSC'15 [15]	ASSCC'19 [16]
Architecture	**SSPLL**	SSPLL	SSPLL	SSPLL
Technology	**22 nm**	40 nm	40 nm	65 nm
Ref. Frequency (MHz)	**1000**	200	40	50
Frequency Range (GHz)	**54 – 60**	12 – 16	53.3 – 63.3	55.5 – 62
PN @ 1 MHz (dBc/Hz)	**−127**	−115	−92	−95
Integrated Jitter[1] (fs)	**19**[2]	56[2]	200[2]	236[3]
Reference Spurs (dBc)	**−39**	−72	−40	−52
Power (mW)	**32**	7.2	42	23
FoM[4]	**−259**	−256	−208	−239

[1] $J_{\mathrm{RMS}} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2}\mathcal{L}(f)\,\mathrm{d}f}$ [17]
[2] Range: 1 kHz – 1 GHz [3] Range: 1 kHz – 100 MHz
[4] $\mathrm{FoM} = 20\log_{10}(J_{\mathrm{RMS}}/1\,\mathrm{s}) + 10\log_{10}(P_{\mathrm{DC}}/1\,\mathrm{mW})$

IV. Conclusion

This paper presents a 56 GHz sub-sampling phase-locked loop for use in a 112 Gbit/s optical transceivers. The voltage-controlled oscillator uses a specialized combined resonator for highest phase noise performance with $\mathcal{L} = -93$ dBc/Hz at an offset frequency of 1 MHz. The loop bandwidth is around 100 MHz for optimizing the noise partitioning between the in-band and the out-of-band phase noise. The frequency locking is implemented with three by-two and one by-seven frequency dividers, a classical phase-frequency detector with dead zone and a specialized digital counter for controlling the four frequency calibration bits of the oscillator. The sampler and the charge pump both have a dummy input to reduce reference spurs. The integrated jitter (10 kHz to 1 GHz) amounts to 18.5 fs, the phase noise at an offset frequency of 1 MHz is −127 dBc/Hz. The resulting Figure-of-Merit (FoM) [13] is an outstanding −259 dB.

Table I shows the comparison with other state-of-the-art PLL implementations, where the proposed work shows a very competitive design. A tape-out of the SSPLL is preparation.

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