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A Divider-less General PLL Lock Assist and Automatic Frequency Calibration System for Millimeter-Wave Sub-Sampling Phase-Locked Loops

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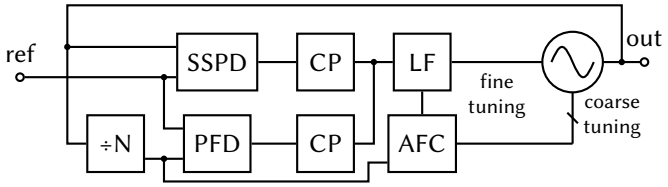
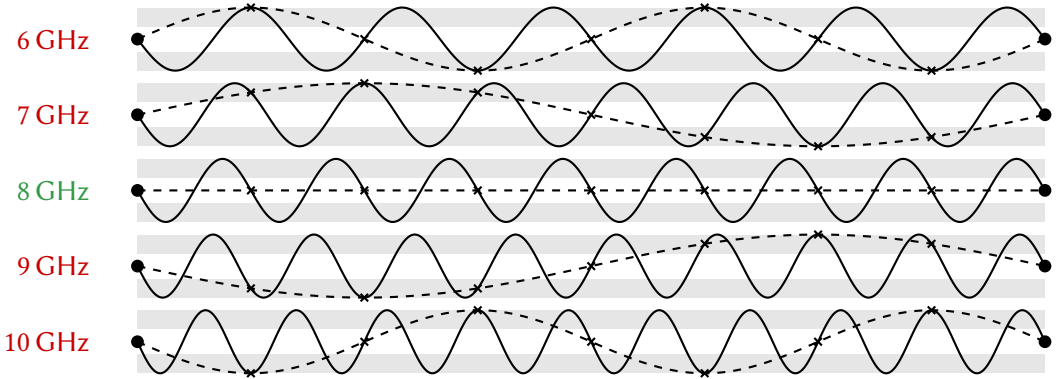
Sub-Sampling Phase-Locked Loops Advantages and Issues



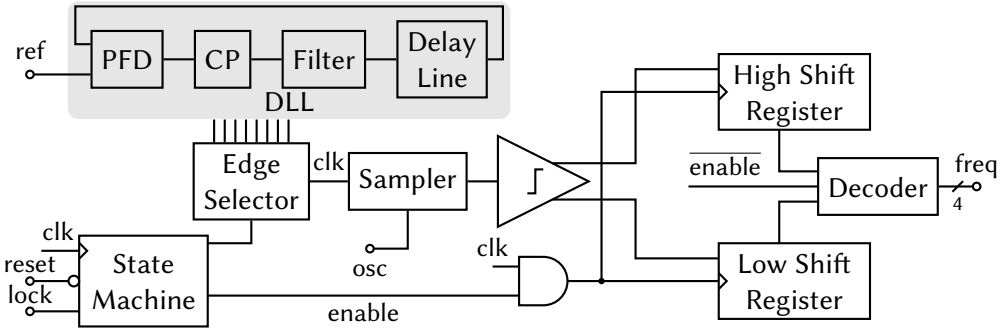
- Sub-sampling phase-locked loop for best jitter performance (no multiplication of loop noise by N^2)
- No power-hungry and bulky feed-back frequency divider
- Sub-sampling phase detector with limited lock-in range
- Can not distinguish between integer multiples of the reference frequency (aliasing)
- SSPLLs employ secondary charge pump phase-locked loop with frequency divider
- Small SSPLL with more efficient and smaller frequency correction desirable

Previous Work



- Divider-less automatic frequency calibration for sub-sampling phase-locked loops
- Virtually raise sampling rate by using N_{aux} auxiliary samples
- Serialized sub-sampling to detect actual lock-in frequency (no aliasing)

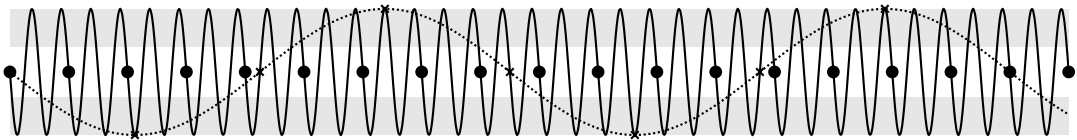
Issues with previous Implementation



- Partly analog processing (lock detector stores values on capacitors)
- Clock generator is complex and poses timing-problem
- Increased sample clock frequency: $f_{\mathrm{clk}} = f_{\mathrm{ref}} \cdot (N_{\mathrm{aux}} + 1)/N_{\mathrm{aux}}$
- No solution for lock-in problem

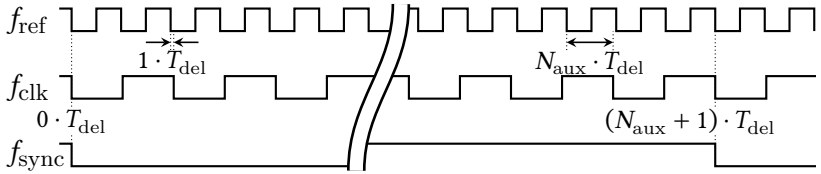
Sub-Sampling Frequency Detection

- Auxiliary samples can be acquired arbitrarily slow
- Generalized expression for required clock frequency: $f_{\mathrm{clk}} = f_{\mathrm{ref}} \cdot \dfrac{N_{\mathrm{aux}} + 1}{1 + k(N_{\mathrm{aux}} + 1)}$
- Sub-sampling factor k can be any positive integer, it can also be altered dynamically
- Previous implementation is similar to $k = 1$ for reasonable values of N_{aux}

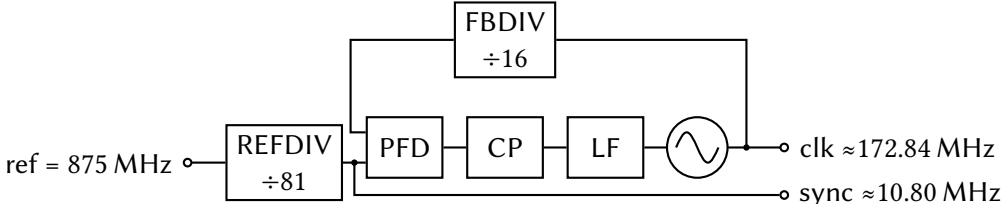


Required Clocks

- Need auxiliary sample clock (clk) and synchronization clock (sync)



- Fractional-N ratio between f_{ref} and f_{clk} required
- Use integer-N charge-pump PLL with two dividers to generate clocks



Noise Analysis

- Auxiliary CPPLL creates noisy clock for AFC
- Worst-case sampling point at zero crossings
- Error must be smaller than ADC resolution:

$$2\pi A_0 f_{\mathrm{osc}} T_J < \frac{A_0}{2^{N_{\mathrm{ADC}}}} \Leftrightarrow T_J < \frac{1}{2^{N_{\mathrm{ADC}}+1}\pi f_{\mathrm{osc}}}$$

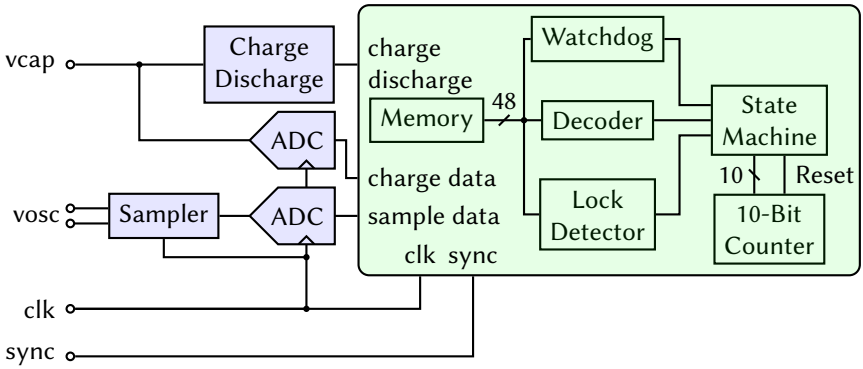
- Leads to jitter requirement of 500 fs
- Phase noise lower integration bound determined by number of samples N_{aux}:

$$f_{\mathrm{lower}} = f_{\mathrm{clk}}/N_{\mathrm{aux}} \approx 11.3\,\mathrm{MHz}$$

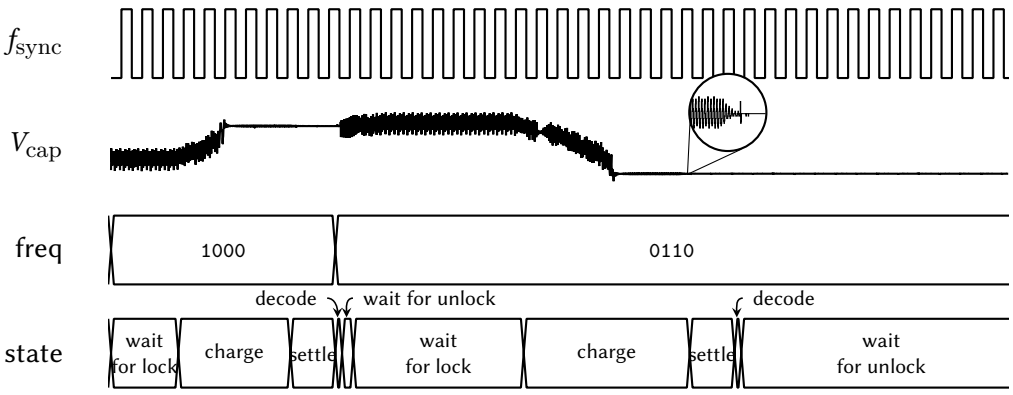
- Estimation and integration of CPPLL phase noise
  $\Rightarrow$ oscillator FoM of -160 dB leads to DC power of 1.77 mW
- Easy to achieve with ring oscillator

Top-level System

- vcap and vosc from main PLL
- small analog front-end with robust digital processing



Simulated Signals



Comparison with State-of-the-Art

Work	JSSC 55/2020	JSSC 49/2014	TMTT 69/2021	This work
Technology (nm)	40	180	65	22 (FDSOI)
Frequency (GHz)	14	2.3	40.5	56
Reference Frequency (GHz)	200	48	100	875
Methodology	FLL	FLL + Counter	Secondary PLL	Sub-sampling with PLL
FLL/AFC DC Power (mW)	1.5	46.7[$]	4.59	1.8
Divider	÷ 70	÷ 2	none	none
AFC/FLL Area (μm^2)	8600[*]	35 600[*]	33 600[*]	4000[#]

[$]Total PLL [*]Estimated from die photograph [#]Pre-layout estimation

Conclusion

- Divider-less automatic frequency calibration for sub-sampling phase-locked loops
- Suitable for highest frequencies, enables truly divider-less millimeter-wave SSPLLs
- Small analog front-end, all processing done in digital
- Most complex block: low-frequency charge-pump PLL with relaxed noise requirements
- Low power and area
- Power consumption can be reduced even further after initial lock (dynamic switching of k)

Thank you for your attention.
Questions?