A Divider-less General PLL Lock Assist and Automatic Frequency Calibration System for Millimeter-Wave Sub-Sampling Phase-Locked Loops

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***Abstract*—In this paper, a truly divider-less, robust and highly configurable lock assist and automatic frequency calibration (AFC) for sub-sampling phase-locked loops (SSPLL) is demonstrated. The design uses a secondary, low-frequency ring-oscillator charge-pump PLL and exploits shifted-phase sub-sampling to obtain frequency information. A fractional ratio between the reference clock of the 56 GHz SSPLL and the sample clock of the AFC is leveraged to achieve sub-harmonic and arbitrary slow frequency detection. Apart from the analog front-end with a high-speed track-and-hold and a simple low-speed, low-resolution analog-to-digital converter, the entire lock detection, frequency processing and calibration is implemented as digital logic.**

***Index Terms*—Sub-Sampling Phase-Locked Loop, Automatic Frequency Calibration, Lock Assist**

I. Introduction

High-performance communications systems for standards with stringent requirements such as 5G, where high frequencies, high resolution and preferably low power consumption are needed, heavily rely on precise phase-locked loops (PLLs). The ubiquitous type-II charge-pump PLL (CPPLL) provides reliable phase/frequency control over a wide operating range (e.g. temperature, process and voltage variations) due to its typical phase-frequency phase detector (PFD). It is, however, left behind noise-wise by injection-locked PLLs or sub-sampling phase-locked loops (SSPLL) [1], both of which need more complex frequency controlling circuits. In SSPLLs usually a regular CPPLL is employed for frequency control and extension of lock-in range, which requires a frequency divider. It is usually very large (as large as an entire oscillator), power hungry and difficult to design. Since the secondary CPPLL is only needed for frequency control, other techniques enable divider-less SSPLL designs with equal noise performance.

A previous work by us [2] employs a delayed sub-sampling approach. This method is effective, but makes use of high frequencies and analog-domain processing, which inhibits further optimization and implementation in newer technology nodes. In this work we will demonstrate some significant enhancements of the original circuit as well as important functional additions to arrive at a fully divider-less frequency control system for SSPLLs. Apart from the analog front-end, all processing is implemented entirely as digital circuit to improve technology scaling and immunity to variations and noise.

This paper will initially focus on the implemented enhancements to the original circuits by explaining the theory first and the implementation details second. After that, a detailed error analysis with a special focus on noise as well as static errors introduced by delays and process variations will follow. Simulation results will be shown at the end of this paper.

II. Circuit Enhancements

In our previous implementation [2], delayed sampling of the oscillator signal is used to capture a pattern with N_{aux} samples, which is then decoded into the frequency state of the locked SSPLL. This is realized with a sampling clock derived from the reference frequency by a delay-locked loop (DLL) and an edge combiner, which selects the required clock edge from all outputs of the DLL. This implementation needs a clock that is higher in frequency as the reference frequency, furthermore the system makes heavy use of analog processing and does not extend the actual lock-in range of the SSPLL. The system presented in this paper addresses these issues by generalizing the approach and moving to a mainly digital low-frequency implementation. In the following the proposed clocking scheme, a detailed system design description, the lock assist as well as the digital implementation will be discussed.

A. Clock Generation

For the delayed sub-sampling a specific frequency delay is needed, which sets the required resolution of the DLL to at least $T_{\text{ref}}/(N_{\text{aux}}+1)$. Furthermore, the generated clock edges have to be recombined into a clock signal with higher frequency. For SSPLLs with high frequency reference signals (which are beneficial for phase noise), this can be challenging. Once the SSPLL is in lock, the phase information of the periodic output signal can also be obtained by sampling the oscillator signal later, similar to sampling oscilloscopes. Here, the aliased frequency information is collected over several periods of the reference frequency. With N_{aux} samples in k periods, the required delay time and clock frequency can be calculated by:

$$T_{\text{del}} = T_{\text{ref}}\Big(\frac{1}{N_{\text{aux}}+1}+k\Big) = T_{\text{ref}}\frac{1+k(N_{\text{aux}}+1)}{N_{\text{aux}}+1} = \frac{1}{f_{\text{clk}}} \quad (1)$$

This is a generalization of the calculation in [2], where $k = 0$. The principle of this clock generation with $k = 2$ is shown in figure 1. After the aligned rising edge of both f_{ref} and f_{clk}, the next AFC clock occurs T_{del} later. The next edge again occurs T_{del} later as the reference edge, so $2\,T_{\text{del}}$ in total. This

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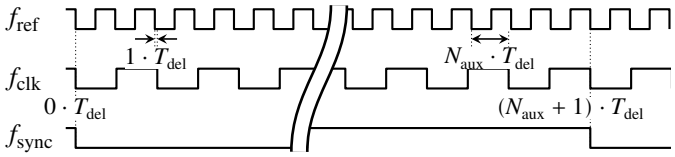

Fig. 1: Principle of the clock generation with $k = 2$

repeats itself with accumulating delay between the edges until $N_{\text{aux}} + 1$ cycles have passed after which the edges align again.

With this configuration, the AFC clock is pseudo-free-running with regard to the reference signal (the AFC can not know the current phase difference of f_{ref} and f_{clk}). For frequency detection it is important to start at the right sample, therefore a synchronization is needed. This can be achieved by a second divided clock, which can be obtained from the AFC clock (also shown in figure 1 as f_{sync}):

$$f_{\text{sync}} = \frac{f_{\text{clk}}}{N_{\text{aux}} + 1} = \frac{f_{\text{ref}}}{1 + k(N_{\text{aux}} + 1)} \tag{2}$$

The required clock f_{clk} can be synthesized by an integer-N PLL with a reference divider for the denominator and a feedback divider for the numerator. The synchronizing clock f_{sync} is then directly provided by the reference divider (see also figure 3). As dividers with odd factors are required, a duty cycle of 50 % is difficult to achieve [3]. However, only the falling edge is critical, since it controls the hold phase of the track-and-hold circuit (TaH). This can also be seen in figure 1 where the position of the rising edge of f_{sync} is unknown.

With equation (1), the required AFC clock frequency can be calculated. How should k be chosen? The clock frequency for the AFC can be arbitrarily low, but this affects the time before the PLL finally locks. The frequency should also not be too high in order to simplify the implementation of the auxiliary PLL and the logic block. In this work it is chosen as $k = 5$, which leads to $f_{\text{clk}} \approx 170\,\text{MHz}$ (with $f_{\text{ref}} = 875\,\text{MHz}$). This is also a reasonable frequency for ring-oscillators.

B. System and Circuit Design

The proposed system is composed of a 56-GHz-SSPLL with an LC oscillator, the AFC and the auxiliary CPPLL generating the necessary clock frequencies for the AFC. The system is depicted in figure 3, where the analog front-end of the AFC is shown in blue and the digital core in green. The AFC uses two low-resolution analog-to-digital converters (ADC) for the samples and the filter voltage to monitor the internal SSPLL state (control voltage, locked state, output frequency). The required resolution of the ADC can be derived from the process of detecting the SSPLL frequency. Three states (low, zero and high) are required, therefore at least two bits are required. In order to have enough margin for noise and mismatch, three bits are chosen. The ADC is implemented as flash-ADC with a fully differential strongARM comparator [2]. As a high-frequency interface, a sampler is needed, which is an exact replica of the main sampler of the sub-sampling phase detector (SSPD) of the SSPLL. Furthermore, a charge/discharge circuit for the SSPLL

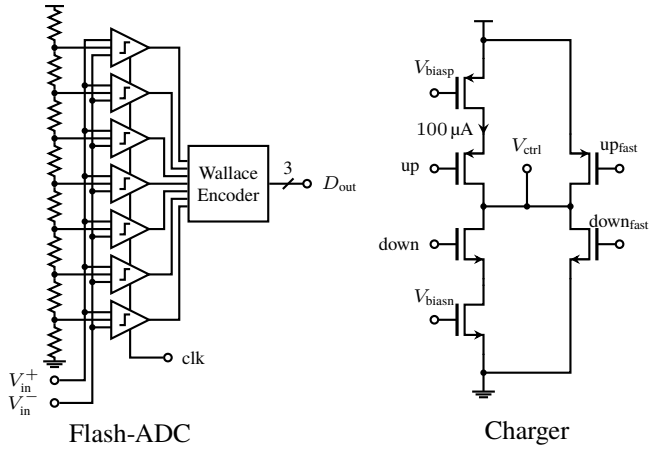

Fig. 2: Circuit implementation of the 3-bit flash-ADC (left) and the SSPLL control voltage capacitor charger (right)

control voltage V_{ctrl} is implemented, which prevents failure of lock and forbidden analog operating points. The charger has a slow- and a fast-charging mode, where the former is controlled by a bias current. The circuit implementations of the ADC and the charger are shown in figure 2.

The required resolution of the ADC is very low and the charger does not require good matching between transistors. Additionally, the digital back-end runs at low frequencies and is designed to equalize setup- and hold-time-constraints to around $1/(2f_{\text{clk}})$. These properties significantly simplify the the design and implementation of both the AFC front- and back-end.

C. Digital System Design

The digital core of the AFC processes the captured frequency and control voltage information. In its main mode (coarse frequency calibration) it waits for the SSPLL to reach a locked state, decodes the frequency information and sets the coarse tuning word of the oscillator accordingly. This repeats until the SSPLL reaches true lock. Since the center frequency of the oscillator roughly follows a normal distribution, the frequency search after decoding the frequency state is not done in a binary-search-manner but rather with increasing distance in the vicinity of the center frequency. The frequency decoder has to be resilient against corrupted samples (through noise, timing mismatch, offset, etc.), which is realized by using an many-to-one look-up table. The allowed budget for clock jitter, ADC noise and other error sources makes this method functional, as the original pattern can always be restored. This is due to the amount of possible patterns ($2^{3 \cdot N_{\text{aux}}}$) versus the number of actual patterns. Additionally the decoder includes a phase-correction to account for static phase offsets.

Besides coarse frequency calibration, the AFC also monitors the fine oscillator control voltage in order to ensure proper analog operating points as well as help the SSPLL to lock. For lock assist, the lock detector monitors consecutive samples (which are equal once the PLL has locked) and counts the number of cycles in which samples are not equal (watchdog). If locking takes too long, the lock assist system gets turned

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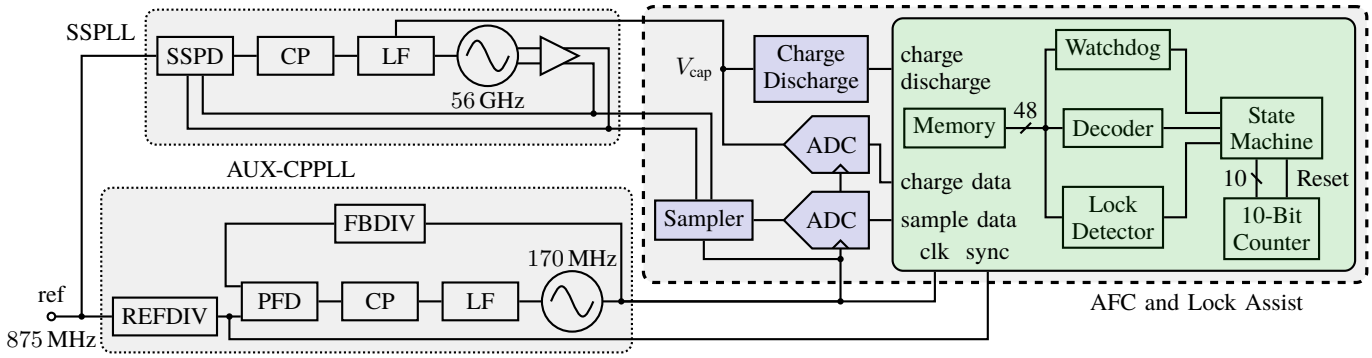

Fig. 3: System Overview of the main SSPLL, the auxiliary CPPLL (both shown on the left) and the AFC. The digital core is shown in green, the analog blocks of the AFC are shown in blue.

on and slowly charges or discharges the main capacitor of the SSPLL loop controller. This helps the PLL to lock faster and extends the lock-in range, as a linear search is performed. If at any stage the control voltage exceeds the allowed voltage bounds (defined by the possible operating voltage of the charge pump and the oscillator), the capacitor is (dis-)charged rapidly until it again reaches allowed voltages.

In order for the AFC to work properly, at start-up or after a reset, the AFC has to (re-)synchronize in order the get the correct phase relationship between f_{ref} and f_{clk} (via f_{sync}). This mode is discussed in more detail in the next section.

III. Noise Analysis and Delay Correction

The proposed AFC uses an auxiliary type-II CPPLL to generate the needed clock signals. As these signals are used to sample the high-frequency output of the oscillator, additional delay between f_{clk} and f_{ref} signal as well as phase noise results in frequency detection errors. Therefore an detailed analysis of the systematic (delay) and the random (noise) errors is necessary.

A. Systematic Errors

Besides the residual CPPLL phase error, additional phase errors are introduced by routing delay, mismatch between the SSPD and the AFC sampler, parasitic devices etc. This causes a shift in the pattern in the AFC, which in turn causes a wrong detection if not corrected. This error can be fixed by using a static offset for the pattern shift. At start-up, this offset is unknown, but it can be determined by the self-calibration mode of the AFC. Here, the PLL is driven into its lowest frequency setting, where the detector can calculate the offset from the difference between the expected and the detected state. Later on this offset is re-used to perform proper frequency calibration.

B. Random Errors

The auxiliary CPPLL and therefore the AFC clock signal exhibit phase noise, which corrupts the samples taken by the AFC. How much noise can be tolerated and is the PLL/oscillator noise critical for this system? The worst-case sampling point is at the zero crossings of the oscillator signal, where the slope of the signal is maximal. However, the zero crossings are not needed for frequency detection in the AFC [2], therefore the jitter requirement can be calculated from a reduced slope. For an SSPLL with a center frequency of 56 GHz with an LC oscillator (with a medium-to-low tuning range, 10 %), only 7 auxiliary samplers (N_{aux}) are needed. This leads to a maximum sample slope of $2\pi A_0 f_{\text{osc}} \cos(\pi/8)$ (given a sinusoidal waveform, which is realistic for mmw PLLs), which can be multiplied with the clock jitter and compared to the threshold of the ADC:

$$\sqrt{2}\pi A_0 f_{\text{osc}} T_J < \frac{A_0}{2^{N_{\text{ADC}}}} \Leftrightarrow T_J < \frac{1}{\sqrt{2}\pi 2^{N_{\text{ADC}}} f_{\text{osc}}} \approx 500\,\text{fs} \quad (3)$$

Equation (3) shows a stringent jitter requirement of only a few hundreds femtoseconds, which calls for a power-hungry low-noise PLL. But this result can greatly be mitigated by considering the phase noise integration bounds: The upper bound is of course infinity, to capture all of the high frequency noise. But the lower bound is set by the number of samples, for which the accumulated jitter has to stay low, which are as few as N_{aux}. After these samples, the auxiliary PLL re-synchronizes the clock with the reference, so the low-frequency noise of these signals is correlated: Jitter in the reference signal slightly shifts the sample in the main sampler of the SSPLL, which is reflected in the samples of the auxiliary sampler. Thus, low-frequency phase noise is of no concern for the AFC. The lower integration bound can then be calculated simply by:

$$f_{\text{lower}} = f_{\text{clk}}/N_{\text{aux}} \approx 11.3\,\text{MHz} \quad (4)$$

The out-of-band phase noise S_ϕ of the PLL is dominated by the VCO and is approximated as a curve with a constant slope of -20 dB/decade (flicker noise will be ignored) and λ_0 as constant: $S_\phi(f) = \lambda_0/f^2$. This simplifies the integration, so that this result can easily be used for the calculation of the required oscillator DC power. The integrated phase noise must be lower than the allowed jitter, as seen in (5):

$$\sqrt{\frac{2\lambda_0}{(2\pi f_{\text{clk}})^2} \int_{f_{\text{lower}}}^{\infty} \frac{1}{f^2} df} < \frac{1}{\sqrt{2}\pi 2^{N_{\text{ADC}}} f_{\text{osc}}} \quad (5)$$

With this expression solved for λ_0, the phase noise in dB can be calculated, then the required DC power of the VCO of the auxiliary PLL can be derived from the FoM. With a typical Figure-of-Merit (FoM) of -170 dB to -160 dB [4], a

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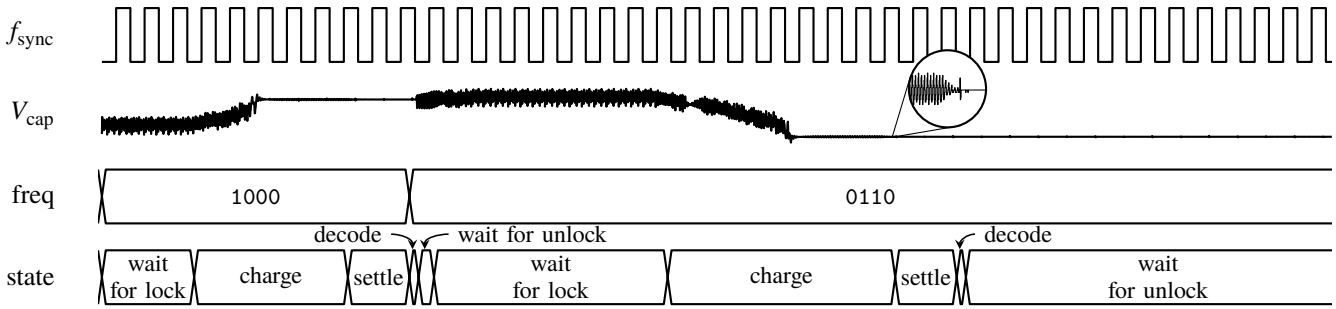

Fig. 4: Circuit-level mixed-signal simulation of the timing- and state-diagram of the AFC digital logic

DC power between 1.77 mW and 177 µW is required. A typical frequency divider for high frequencies already consumes several milliwatts [5], so even a mediocre FoM of −160 dB is feasible.

IV. Simulation Results

The entire system was implemented in a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology and simulated on circuit-level (mixed-signal simulation). Figure 4 shows important/relevant signals of the system: The filter capacitor voltage alongside the internal control state, the coarse frequency setting and the synchronizing clock as a time reference. As can be seen, the limited lock-in range prevents the SSPLL from reaching a locked state, therefore the lock-assist system starts slowly charging the capacitor, which eventually helps the SSPLL to lock. After charging was active, the SSPLL returns to run disturbance-free, without any charging. Since the sample values change in this period (due to the time constant of the SSPLL filter), the AFC has to wait for the settling. The zoomed-in plot shows the settling of the tuning voltage. After this, the frequency state is decoded and the coarse frequency tuning updated. After the second time, the SSPLL is in true lock and the AFC stays idle until unlocked again.

V. Conclusion

In this paper a comprehensive system for SSPLL lock assist, automatic frequency calibration and oscillator control voltage monitoring is demonstrated. The frequency of the SSPLL in lock is calculated from (arbitrary slowly) sub-sampled, digitized values and accordingly updated. Additionally, the lock-in range is increased and the total lock time reduced. Apart from the analog front-end, all signal processing is implemented as digital circuit, accompanied by a low-resolution ADC and a replica of the SSPD. The proposed AFC enables precise frequency control and is robust against process variation by using self-calibration. The power consumption of the system amounts to 1.8 mW and is mainly spent in the CPPLL/VCO (400 µW), the digital core (850 µW) and the ADCs (250 µW each). Table I shows the comparison of the proposed system with other related work. Our work is the most efficient implementation regarding area and power consumption and is applicable to virtually any PLL configuration by appropriate adaption of N_{aux} and the divider values of the auxiliary PLL.

TABLE I: Comparison with State-of-the-Art

Work	[6]	[7]	[8]	This work
Technology (nm)	40	180	65	22 (FDSOI)
Frequency (GHz)	14	2.3	40.5	56
Reference Frequency (GHz)	200	48	100	875
Methodology	FLL	FLL + Counter	Secondary PLL	Sub-sampling with PLL
FLL/AFC DC Power (mW)	1.5	46.7$^{\$}$	4.59	1.8
Divider	÷ 70	÷ 2	none	none
AFC/FLL Area (µm^2)	8600*	35 600*	33 600*	4000$^{\#}$

$^{\$}$Total PLL *Estimated from die photograph $^{\#}$Pre-layout estimation

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