A Transmission-Line-based Phase Shifter for High-Speed, Ultra-Low-Power N-PSK Transmitters

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***Abstract*—This paper presents a transmission-line-based phase shifter for use in a PSK/APSK ultra-low-power transmitter. In upcoming extreme high-data-rate communications standards, the power consumption of complex digital-to-analog converters will dominate the total power consumption. Therefore, other means have to be found to enable complex modulation schemes while providing high power efficiency. The proposed phase shifter implements a switched delay with only switching transistors and a transmission line, making this a very energy-saving design. It can be applied to any N-PSK modulation with bit depth N by configuring the transmission line length via selecting the appropriate switches. Furthermore, several different modulation depths can be implemented on one chip by using only a set of switches. The design in a 22 nm FDSOI node shows feasibility of the proposed approach with successful QPSK and 8-PSK modulation at 56 GHz and 28 GHz, respectively.**

I. Introduction

In recent years, the power consumption of analog-to-digital converters (ADCs) for receivers and digital-to-analog converters (DACs) for transmitters started to dominate the total power consumption of transceiver architectures, especially for highest data rates (with high modulation depths). This poses a significant challenge for mobile devices, where high-speed communication should not impede long battery life, let alone the ecological impact. For many high-density communication standards, quadrature-amplitude modulation (QAM) is the predominant modulation format to achieve high spectral efficiency. This comes at the cost of high-power data converters. A different, also popular modulation scheme is phase-shift keying (PSK) or amplitude-phase-shift keying (APSK), which are beneficial in terms of detection range (e.g. signal-to-quantization-noise ratio, SQNR) at the receiver side for signals which high peak-to-average power ratio (PAPR) [1].

Traditionally, standard transmitters and receivers are built using an in-phase (I) and a quadrature (Q) path to upload the data onto the carrier, via a frequency mixer. In recent years direct-RF or digital transceiver techniques have emerged, where the data directly modulates the carrier, without any required mixers or linear combiners. This has advantages for the calibration and configuration of the transceivers (e.g. for multi-standard purposes), but requires data converters running at carrier frequencies, up to several GHz, with a corresponding tremendous power consumption [2]. A different architectural approach for transceivers are polar systems, where amplitude and phase of the carrier signal get modulated independently. While digital polar transmitters have been around for a while [3], most of the time they are used to realize cartesian modulation (e.g. QAM). With the emerge of true polar receivers such as [4], direct-RF techniques can be combined with sub-sampling polar transceiver methods to arrive at ultra-efficient communication systems with high data throughput and increased power efficiency, as polar receivers are generally better suited for signals with a non-uniform signal probability distribution, such as in orthogonal frequency-division multiplexing (OFDM) [5].

Polar transmitters are implemented with phase-locked loops (PLL) that allow phase modulation, for example with two-point modulation [6]. This enables low-power polar transmitters, but even better power efficiency can be achieved with a very simple PLL followed by a phase shifter, which can be implemented with passive structures, especially for high frequencies [7]. This is especially interesting as with increasing carrier frequencies passive structures such as transmission-line filters or antennas can be implemented on-chip with a reasonable size [8], replacing a more complex system assembly, thus reducing cost. Therefore the design of passive components and system architectures based on them will become even more important for future networking applications requiring both highest data rates and lowest power consumption.

This paper proposes a passive transmission-line-based phase shifter with multiple output phases based on a series of elementary phase-shifting elements. It can be used used for various polar modulation formats (with constant phase difference such as in QPSK) in a direct-RF polar transmitter. This greatly simplifies transmitter design, as no DAC, no mixer and no multi-phase clock is needed. This approach enables ultra-low power integrated transmitters for highest data rates. The work is organized as follows: In section II the implementation of the phase shifter and some design issues are discussed. Section III shows and discussed the simulation results and finally we will conclude the findings in section IV.

II. Phase Shifter Implementation

A. General Design

The design of the phase shifter is greatly motivated by the architecture of a direct-RF polar transmitter. Figure 1 shows the architecture of the phase-shifter-based transmitter. It is comprised of a periodic signal generator (e.g. a phase-locked loop), the phase shifter, a power amplifier (PA) and the antenna (or some other connection to the channel). The

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digital data is directly fed into the phase shifter, operating at carrier frequencies. Therefore this a mixer-less transmitter, also called direct-RF or digital transmitter. The comparison

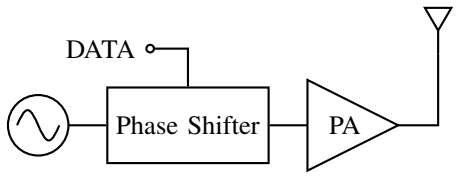

Fig. 1: Architecture of a phase-shifter-based N-PSK transmitter

to the traditional QPSK transmitter shows a greatly simplified architecture without any required mixers, digital-to-analog converters, linear power combiners and quadrature signals. It consists of a long winded transmission line with the phase-shifted output at the right side.

The phase shifter is a series combination of individual phase-shifting elements (PSE), which are for this work simply transmission lines with lengths of $\lambda/4$, $\lambda/8$ etc. The PSE is realized by a co-planar wave guide (CPWG) with a geometry matching a characteristic impedance of 50 Ω. Figure 2 shows the concept of the phase shifter. The carrier signal (coming

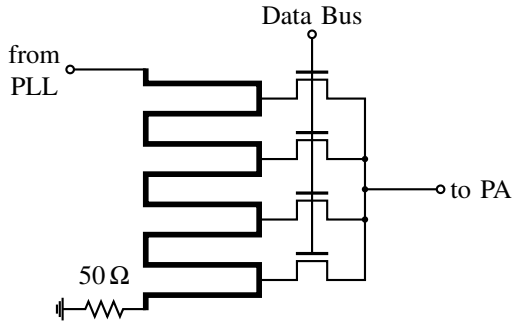

Fig. 2: Phase Shifter Concept

from a PLL) is fed into the phase shifter, comprised of four segments. The transmission line is terminated with 50 Ω at the end. The middle of each segment can be selected by enabling the corresponding switch. The output signals are then combined and amplified by the power amplifier of the transmitter. This is done by a passive linear power combiner, such as a Wilkinson combiner [9]. We used a simple summing tree for the demonstration of the overall concept. The lengths of the transmission lines are matched to each other in order to prevent any further phase shifts.

As the transmission line is terminated with 50 Ω, the reflections are minimized. However, the parasitic capacitances (a few femto farad) of the switches load the transmission line and lead to slight mismatches in the characteristic impedance. As the available area for further matching components such as open/short stubs or inductors is scarce, a sensible matching network for the switches is not feasible. The slight degradation of the reflection is still within acceptable range for the phase modulator.

Figure 3 shows the layout of the proposed phase shifter. The transmission lines are bent in order to realize a more equalized width and height of the structure. The switches are situated in the middle of the bends, right underneath the signal lines. The transmission lines are laid out as co-planar wave-guides (topmetal in purple) and the entire area is supported by a metal shield on a low metal (orange shapes). The required chip area of the entire phase shifter (without saturating amplifier and carrier generator) is 325 µm × 165 µm, which corresponds to less then 1 % of a die with a size of 2.5 mm × 2.5 mm and is therefor reasonable to implement.

B. Wide-Band Operation and Modulation Depth

A transmission-line-based phase shifter consumes virtually no power and is easy to implement. However, it is only operational (with acceptable phase error) for a very narrow range of carrier frequencies. Since the physical size of such a phase shifter is quite large, it is not feasible to integrate an array of phase shifters with different lengths of the transmission lines, therefore other means have to be found to implement wide-band operation. We propose an array of switches distributed along the entire transmission line that are configured to match the carrier frequency. A digital configuration block together with logica gates selects the correct switches for the transmitter.

The length L_t of the PSE can be derived from the minimum needed phase shift $\Delta\varphi$ and the wavelength λ_c of the carrier signal (56 GHz in this work). The minimum needed phase shift depends on the number of bits $N_{\max}$ of the modulation format (e.g. two for QPSK, three for 8-PSK).

$$L_t = \frac{1}{2^{N_{\max}}} \cdot \frac{c_0}{f_{c,\max} \cdot \sqrt{\varepsilon_r}} \tag{1}$$

A QPSK modulator for example needs phase differences of 90°, which corresponds to a quarter of the carrier wavelength.

Besides the consideration of carrier frequencies and needed modulation depths the transmission lines can be replaced by wide-band phase shifters, for example based on stub-loaded transmission lines [10] or tuned transmission lines [11]. This maintains the simplicity of the overall design and adapts the transmitter to a broader range of possible carrier frequencies.

In order to support different carrier frequencies and modulation formats, the output switches of the phase shifter need to be enabled/disabled, according to the configuration setting. A simple scheme similar to row/column select in digital memories can be used. Figure 4 shows three example configurations: Full-rate QPSK (where the full-rate is the maximum possible carrier frequency), half-rate QPSK and half-rate 8-PSK. A modulation order higher than QPSK (or 4-PSK) is only possible for carrier frequencies lower than the full rate. For the half rate, each transmission line segment shifts the phase by 45°, therefor 8 segments are needed for full 360°. This can be used to implement 8-PSK, or QPSK, if only every second switch is enabled (as shown in figure 4). The full rate needs only the first four segments, so all subsequent switches are unused. This scheme can be extended in order to support, for example, 16-PSK at quarter rates. The limiting factor then is the physical

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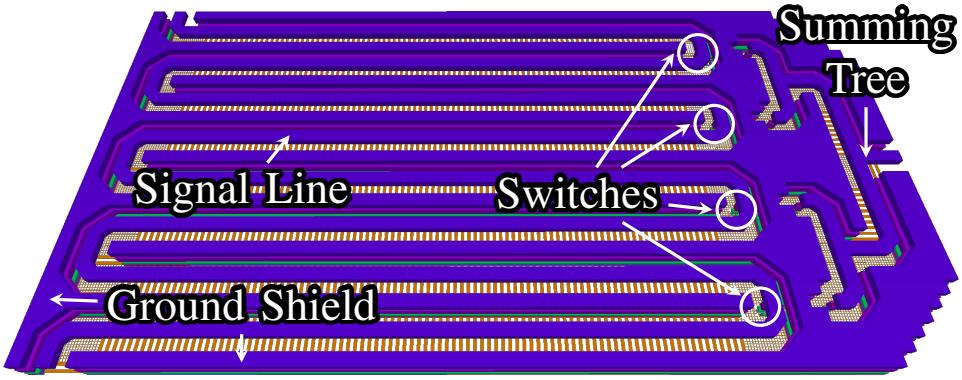

Fig. 3: Layout of the proposed transmission-line-based phase shifter. The signal is fed in on the top left, at the bottom left the termination is placed. The right part shows the summing tree, which is then fed into the saturating amplifier. The lower-metal ground grid covering the entire structure is displayed in orange, the signal lines in dark purple.

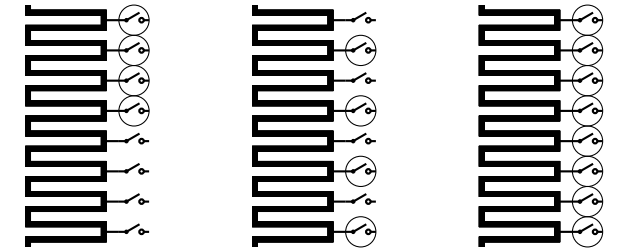

Fig. 4: Example of possible switch configurations

on-chip area of the phase shifter. The gate signal selectors for the switches are simple logical-AND gates. Depending on the number of switches, several signal lines have to be routed to the cells. As there is strong ground plane around the phase shifter signal lines, the gate signals can safely be placed in lower metal layers without any significant impact on the overall RF performance of the phase shifter.

C. Power Amplifier and Amplitude Variation

The power amplifier of the transmitter drives the antenna and raises the power level for transmission. In general, modulation formats with amplitude information (QAM, ASK, APSK) need linear power amplifiers as otherwise the non-linearity would deteriorate the data. However, phase or frequency modulation formats do not suffer from this and can use highly non-linear power amplifiers. This has the benefit of higher power efficiency [3], [12], as PAs have a significant impact on system power consumption, especially at high back-off power in more linear operation regions. The non-linearity of these amplifiers can also be exploited as useful property, namely for compressing the signal and removing any unwanted amplitude modulation. These can occur due to non-perfect impedance matching of the transmission lines and the switching action, leading to a data-dependent amplitude of the output signal. Since the antenna and the matching network have a resonating characteristic, any harmonics are heavily filtered before reaching the channel.

III. Simulation Results

The proposed phase shifter was implemented in a 22 nm FDSOI technology with a metal stack with RF capabilities (high-Q thick copper), although other technologies are possible. The transmission lines and the summing tree have been simulated electro-magnetically (EM) with Keysight ADS. The resulting S-parameters were combined with transistor models for the switching and appropriate termination resistors. For the saturating amplifier a behavioral model based on Verilog-A was used, which realizes a tanh-characteristic.

Figure 5 shows the simulated S-parameters of the individual transmission line segments with 90° phase shift. They have practically no loss (because of the high-Q metal) and sufficient

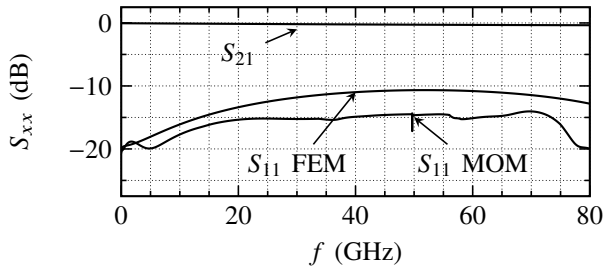

Fig. 5: Simulated S-parameters (transmission/reflection) of a single segment with the foundry-provivded substrate

low reflection. The lines were simulated with both the moment of methods (MOM) and the finite-elements method (FEM) for increased accuracy and comparison. Both simulation results are in perfect accordance with each other for S_{21} and show only small differences for S_{11}. Overall the MOM results show some simulation artifacts so the results from the FEM simulation are used for further system simulations.

The entire phase shifter with summing trees and saturating-amplifier model was used as PSK modulator for a corresponding transmitter. The ideal input signal has a frequency of 56 GHz and an amplitude of 1 V, the data rate is 1 GHz. Figure 6 shows the simulated waveforms of the phase shifter. The power

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amplifier removes the amplitude variation but keeps the phase modulation, shown in the lower graph. The upper graph plots

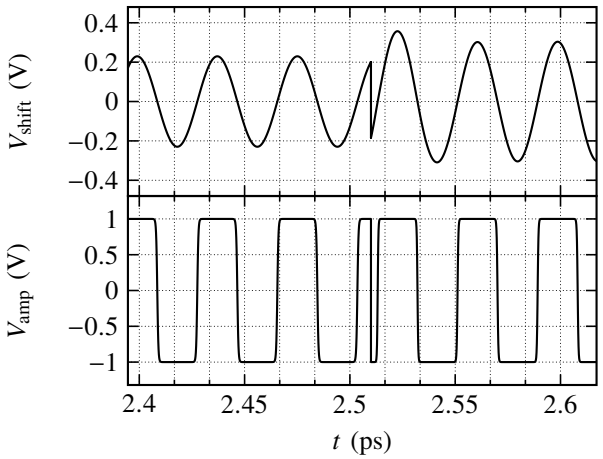
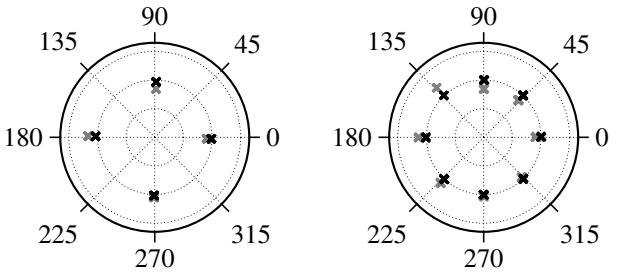


Fig. 6: Simulated waveforms before (top) and after (bottom) the power amplifier

the output signal of the phase shifter before the power amplifier, displaying significant amplitude variation (about 30 %).

Figure 7 shows the simulated constellation diagram of the proposed transmitter at full-rate QPSK and half-rate 8-PSK before (gray) and after (black) the power amplifier. A pseudo-



(a) Full-Rate QPSK (56 GHz) (b) Half-Rate 8-PSK (28 GHz)

Fig. 7: Simulated normalized constellation diagram of the phase modulator at different modulation settings and carrier frequencies. Black marks are after the power amplifier, gray marks before

random bit-stream (PRBS) was used as data source. Both constellation data are normalized for better comparison. The power amplifier filters out the amplitude information so that all constellations lie on the unit circle. The phase shifter precisely generates all needed phase constellations with high precision.

IV. Conclusion

In this paper, a concept for a passive transmission-line-based phase modulator for direct-RF transmitters is presented. It can be used together with a fixed-frequency oscillator (PLL) and a power amplifier to build a full transmitter, consuming only minimum power. The concept of the phase shifter allows for a wide range of carrier frequencies as well as different modulation depths (regular PSK, QPSK and higher N-PSK) by using a complex configuration block to enable the needed switches together with matching carrier frequencies. Furthermore, with the emergence of digital power amplifiers, an ultra-low-power direct-RF polar APSK transmitter can be realized. The transmission lines can be laid out regarding the minimum carrier frequency to be supported, with simple modification possibilities. The individual phase-shifted signals are combined by a linear passive power combiner. Any occurring amplitude variation is filtered out by the use of a highly non-linear power amplifier. The overall system study shows promising results for low power transmitters at high frequencies and data rates.

Acknowledgment

The authors would like to thank GLOBALFOUNDRIES for the University Multi Project Wafer Program and the BMBF (German Ministry for Education and Research) for funding this work within the *fast* initiative as well as Ravi Subramanian and Mentor for Analog FastSPICE (AFS) support.

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