A 0.007 mm^2 48 – 53 GHz Low-Noise LC-Oscillator using an Ultra-Compact High-Q Resonator

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Introduction

Motivation

- Communication links: high data rates require low noise local oscillators
- On-chip VCOs are significant phase noise contributors
- State-of-the-art low noise oscillators: based on LC-resonators
- Power consumption of clock generators will explode in near future (see "Jitter-Power Trade-Offs in PLLs", Behzad Razavi, TCAS I April 2021)
- LC-resonator-based oscillator are good, but not good enough

Application

- Clock generators for high-speed optical transceiver (data rates of around 100 Gbit/s)
- Pulse-Amplitude-Modulation with four levels (PAM-4) → clock frequency of 50 GHz

Optimized Resonator Design

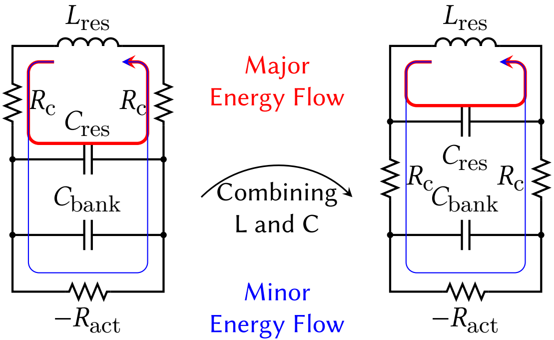
- Leeson's renownded equation for oscillator phase noise:

$$S_\phi(\Delta\omega) = \left(\frac{2FkT}{P_S} + \frac{\alpha}{\Delta\omega}\right)\left(1 + \left(\frac{\omega_0}{2Q_{\mathrm{res}}\Delta\omega}\right)^2\right)$$

$$\approx \left(\frac{2FkT}{P_S} + \frac{\alpha}{\Delta\omega}\right)\left(\frac{\omega_0}{2Q_{\mathrm{res}}\Delta\omega}\right)^2 \propto \frac{1}{Q_{\mathrm{res}}^2}$$

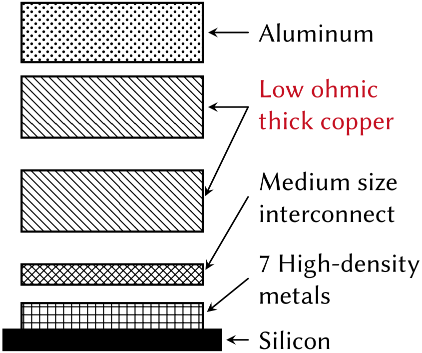
- Noise scaled by resonator Q (noise floor only reached at very high offset frequencies)
- Integrated LC-resonators don't offer too much Q-factor (usually around $10 - 30$)
- Optimizing electro-magnetical resonator structure for higher Q

LC Resonator Interconnect Resistance



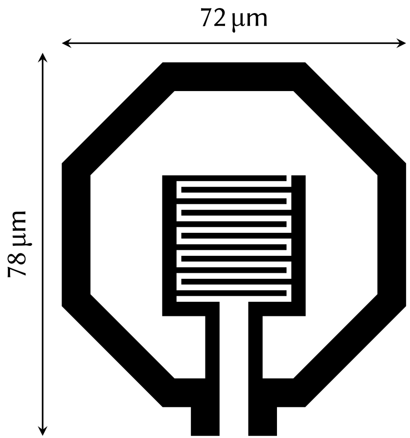
- LC resonator looses only little energy in one cycle
- Conncetion between L and C: needs to pass through many vias (almost entire metal stack)
- Eliminate interconnection resistance by merging L and C on high RF metal
- Only minor energy flow to capacitive bank and active circuitry

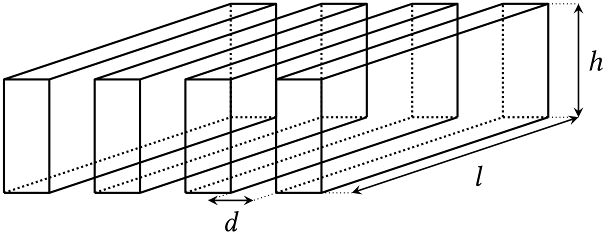
Technology Metal Stack



- Technology: 22 nm FDSOI
- 11 metals, with Low ohmic copper perfect for RF passive devices
- Top-level aluminum used for power grid, less suitable for RF applications
- Vastly reduced capacitor finger density on high metals (approximately $10\,\mathrm{nm}^{-1}$ vs. $0.2\,\mu\mathrm{m}^{-1}$)
- Much higher capacitance between fingers due to high side walls

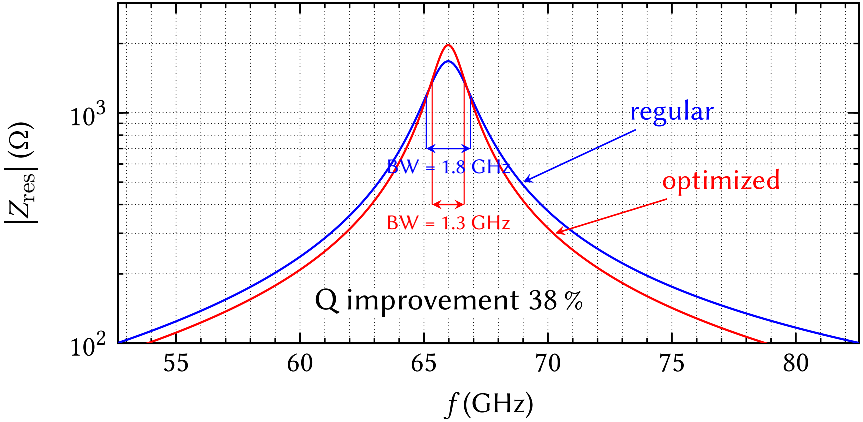
Resonator Layout





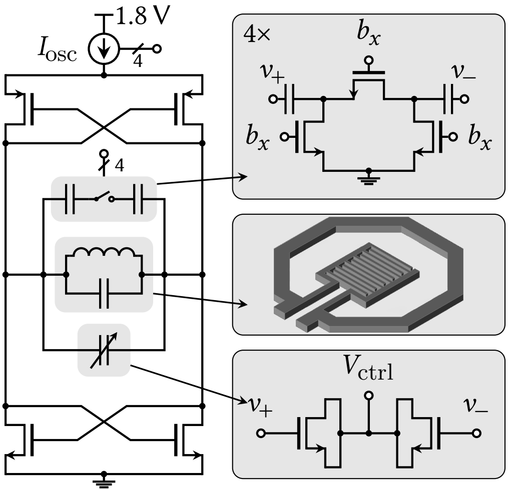
- Pitch of capacitor fingers: 2.4 µm (50 % density)
- Simple parallel-plate capacitor as rough estimate:
  $C = \varepsilon_0 \varepsilon_r \cdot N \cdot A/d = \varepsilon_0 \varepsilon_r \cdot N \cdot h \cdot l/d \approx 35\,\text{fF}$
- Actual capacitance higher due to more complex electrical field
- Capacitor fills inductor → No toplevel fill required

Optimized Resonator Design – Q-Factor Improvement



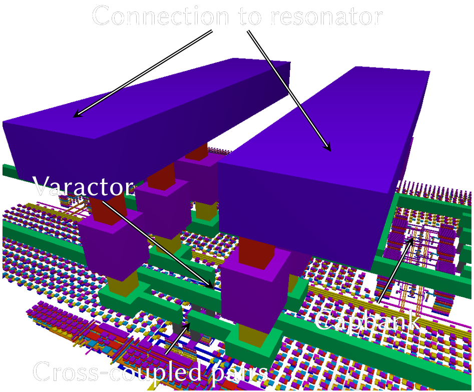
- Comparison between optimized (red) and regular (blue) resonator
- Capacitors of regular resonator tuned for matching resonance frequencies
- Bandwidth of impedance of optimized resonator slightly but noticable narrower

Overall Oscillator Architecture

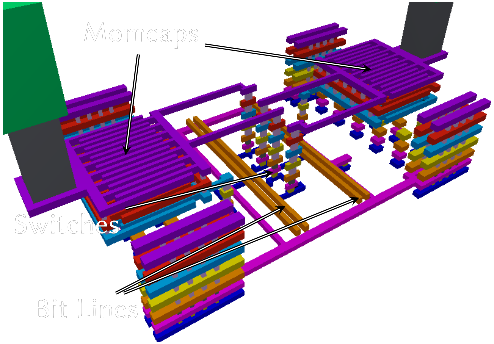


- Two cross-coupled pairs (nMOS & pMOS) for improved signal swing
- nMOS-based varactor for continuous fine tuning (temperature, voltage variations)
- small capacitor bank (4 bits) for discrete coarse tuning (process variations)
- inductance target: 150 pH
- fixed capacitance target: 35 fF
- center frequency without active circuitry and parasitics approximately 70 GHz

Layout Implementation

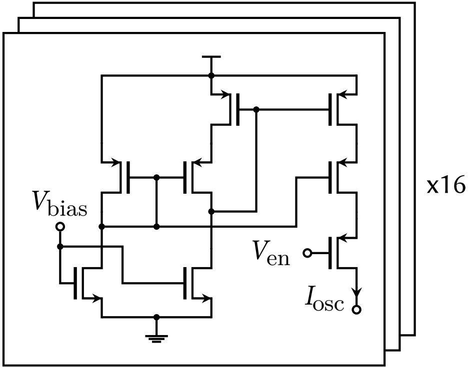


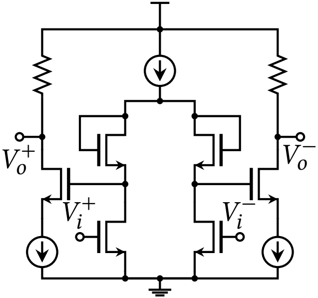
Connector to Resonator



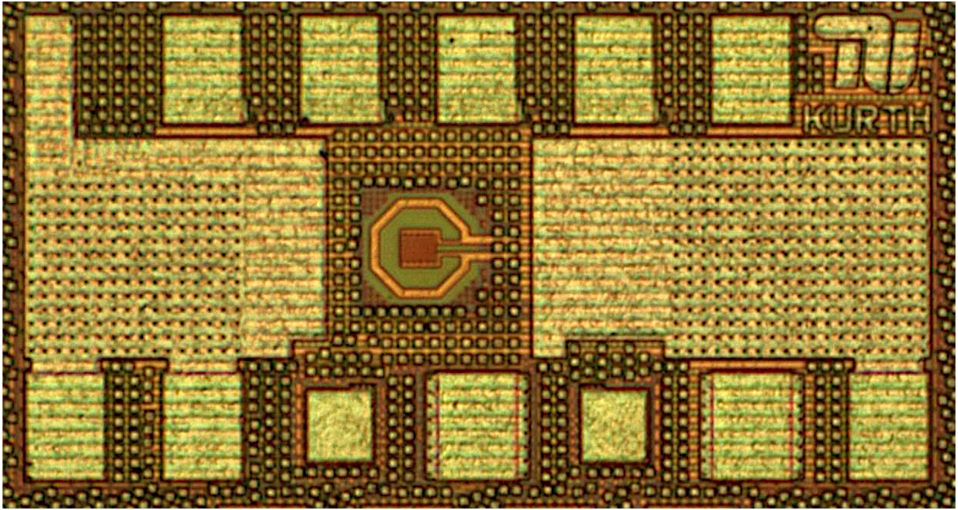
Capacitor Bank Single Bit

Auxiliary Circuits

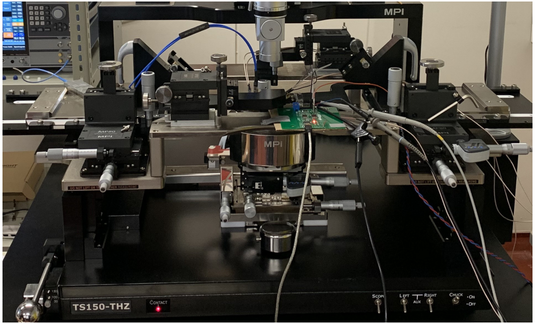


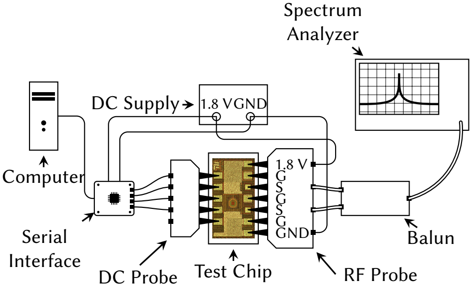


Die Photograph



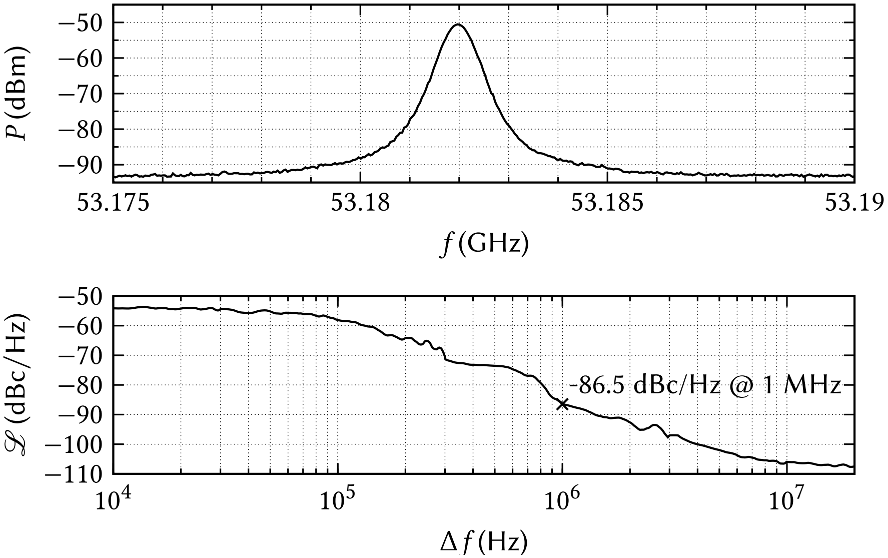
Measurement Setup



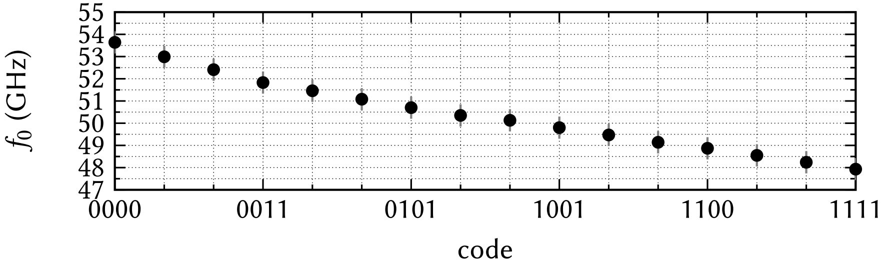


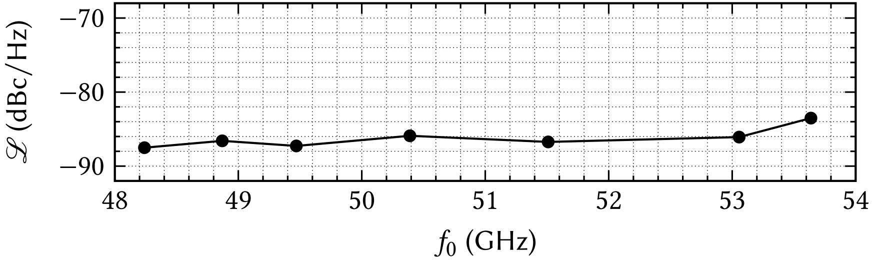
- Oscillator tested on wafer prober
- Measurement setup attenuates signal by more than 26 dB
- Spectrum Analyzer: Rohde&Schwarz FSW67

Measurement Results – Spectrum and Phase Noise



Measurement Results – Tuning





Comparison with State-of-the-Art

	This Work	**ISSCC'20 [1]**	**JSSC'16 [2]**	**MWC-Letters'15 [3]**
Technique	**Optimized LC-resonator**	Current-Output VCO + HCF + Current-Reuse TIA	Harmonic Extraction	Low-Q Series LC Tanks
Technology	**22 nm FDSOI CMOS**	65 nm CMOS	40 nm CMOS	40 nm CMOS
Supply Voltage (V)	**1.8**	0.9	0.7/1	0.9 – 1.1
Power Consumption (mW)	**4.5**	9.0	24.0	8.5 – 16
Output Frequency (GHz)	**53.4**	59.8	55.5	4.97
Phase Noise @ 1 MHz (dBc/Hz)	**–86.5**	−100.7	−100.1	−107
Core Area (mm^2)	**0.007**	0.12	0.13	0.0063
FoM / FoM_A @ 1 MHz (dBc/Hz)	**–175 / –166.1**	−186.7 / −165.9	−181.5 /−160	−170.1 / −162.3

$$\mathrm{FoM} = \mathscr{L}(\Delta f) - 10\log_{10}(f_0/\Delta f) + 10\log_{10}(P_{\mathrm{DC}}/1\,\mathrm{mW})$$
$$\mathrm{FoM_A} = \mathscr{L}(\Delta f) - 10\log_{10}(f_0/\Delta f) + 10\log_{10}(P_{\mathrm{DC}}/1\,\mathrm{mW}) + 10\log_{10}(A/1\,\mathrm{mm}^2)$$

[1] C. Fan, J. Yin, C. Lim *et al.*, "17.9 A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 282–284.

[2] Z. Zong, M. Babaie and R. B. Staszewski, "A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.

[3] M. Tohidian, S. A. Ahmadi-Mehr and R. B. Staszewski, "A Tiny Quadrature Oscillator Using Low-Q Series LC Tanks," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 8, pp. 520–522, 2015.

Thank you for your attention!

Questions?