A 0.007 mm^2 48 – 53 GHz Low-Noise LC-Oscillator using an Ultra-Compact High-Q Resonator

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***Abstract* — This paper presents a 50 GHz LC-oscillator utilizing an ultra-compact merged resonator design obtaining an outstanding low phase noise of −86.5 dBc/Hz at 1 MHz offset while occupying an area of only 0.007 mm^2. The resonator implementation achieves both a high quality factor and metal density error-free design by using a top-metal capacitance structure placed within the 150 pH inductor. This leads to a robust process-tolerant and compact resonator realization. Furthermore, with the inductor and the main capacitor being on the same metal level, the harmful interconnect resistance is eliminated, which further enhances the quality factor. The proposed resonator implementation enables a rapid and reliable LC-oscillator design with improved phase noise in deep nanometer CMOS technologies. Implemented in a 22 nm FDX CMOS technology, the 50 GHz LC-oscillator is tunable between 48 GHz and 53 GHz while consuming only 4.5 mW from a single 1.8 V power supply resulting in an excellent Figure-of-Merit of −175 dBc/Hz.**

***Keywords* — LC oscillator, mm-Wave, SOI CMOS, Resonator**

I. Introduction

Next-generation optical wire-line communication standards aim for 400 Gbps in four lanes of each 100 Gbps (IEEE 802.3bs). For cost-effective solutions, the optical transceivers are built using low-cost vertical cavity surface-emitting lasers (VCSEL) and silicon-based photo diodes with multi-mode fibers and single-chip CMOS transceivers. This needs efficient and low-cost high-precision frequency synthesizers for complex (non-) linear equalization filters with sub-unit-interval taps and clock-and-data-recovery circuits. The oscillator architecture of choice for integrated high-performance phase-locked loops (PLL) are LC-oscillators, as they offer best phase noise performance of all on-chip oscillator topologies.

The limited tuning range of LC-oscillators (compared to ring-oscillators) is no issue in fixed-frequency, integer-N frequency synthesizers as only process/voltage/temperature (PVT) variations need to be compensated. The standard architecture employing a cross-coupled pair has been studied extensively during the last years, resulting in many different circuit techniques for improving important characteristics, such as filtering techniques [1], current reuse [2], active inductors [3] and higher-harmonics extraction [4]. While these are effective methods for reducing phase noise, they increase the circuit complexity and with this the power consumption and the required silicon area, both precious resources in low-cost transceiver systems. High-performance PLLs such as sub-sampling PLLs (SSPLL) with ultra-low in-band noise [5] allow for relaxed oscillator performance, as other noise contributions become equally significant [6]. For cost-efficient systems with a small form factor, there is a demand for LC oscillators with a good area/purity trade-off.

This paper presents a very small (< 0.01 mm^2) LC-Oscillator for use in CMOS transceivers with data rates of over 100 Gbps that enables rapid circuit development cycles, resulting in compact area- and power-efficient designs without the need for complex auxiliary circuits. The proposed oscillator achieves its good area-efficiency by the use of a specialized optimized resonator design for a high quality factor. The work is organized as follows: The introduction is given in section I. In section II the techniques for low-noise mmw-oscillators as well as the actual circuit implementation are discussed. A detailed analysis of the resonator and insight into the design is given in section III. After this, measurement results are provided in section IV and the conclusion in section V.

II. Circuit Techniques and Implementation

Several techniques have been reported for improving oscillator phase noise and power efficiency: In [4] a specialized resonator is used to create an oscillation at two frequencies. A tuned amplifier is then used to amplify only the higher harmonic. The drawback of this design is the enormous power consumption of the required amplifier. A different approach is taken in [7], where a current-output oscillator with large harmonics together with a harmonic-current filter (HCF) is implemented. Following the filter, a trans-impedance amplifier with a resonant tank restores a high signal amplitude. The overall power efficiency is good, but the required area is quite high. A ring-oscillator-like LC-oscillator at 5 GHz is shown in [8], where the individual inverter stages are coupled by low-Q inductors. While this design achieves reasonable phase-noise results, its feasibility at higher frequencies remains to be investigated. Overall, a good compromise between performance, power efficiency and area consumption for RF oscillators is lacking in the current state-the-art.

The proposed oscillator as shown in figure 1 uses a complementary architecture with two cross-coupled pairs (CCP), a high-side pMOS current source, a bank of switched capacitors (capbank) for coarse frequency calibration and a varactor for analog fine tuning. The supply voltage is twice the core voltage of 900 mV for maximizing the oscillator amplitude. The cascoded current mirror has a voltage drop of 900 mV to prevent over-voltage stress of all core devices. The main resonator uses a combined implementation for both the inductor and the main

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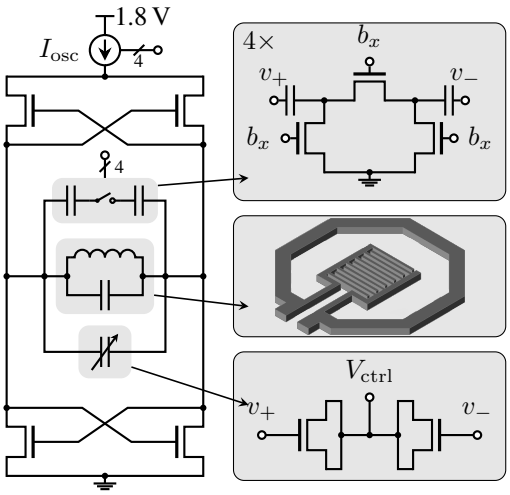

Fig. 1. Top-level architecture of the oscillator with implementations of the individual components

capacitance, where the two components are merged on RF-capable top-metal, leading to a compact and ultra-efficient design. The capbank has four binary-weighted bits with a minimum step size of around 350 MHz, resulting in a tuning range of approximately 5.6 GHz (10 %). The varactor is added for fine frequency tuning for use in an analog SSPLL. As varactors are a significant noise source in oscillators, the fine tuning range is kept small. It is designed to cover two coarse tuning steps, leaving some margin for variation.

III. Resonator

The resonator is the main frequency-defining component in the oscillator and of major importance for the overall purity of the oscillator signal. The quality factor Q_{res} of the resonator governs the minimum phase noise that can be reached as described by Leeson's renowned equation [9]:

$$S_\phi(\Delta\omega) = \left(\frac{2FkT}{P_S} + \frac{\alpha}{\Delta\omega}\right)\left(1 + \left(\frac{\omega_0}{2Q_{\mathrm{res}}\Delta\omega}\right)^2\right) \quad (1)$$

Therefore, the purity of the oscillator is proportional to the loaded quality factor of the resonator. Usually the resistance of the inductor dominates the overall quality factor. Technologies with RF-capable low-ohmic metals offer reasonable quality factors of over 30, but the interconnect resistance between the inductor on top-level metals and the capacitors and active devices on lower metals remains an issue. As shown in figure 2 the main energy of an LC-oscillator is stored in the resonator, the amount of current going through the rest of the circuit is far lower than the current within the resonator. The main elements are the inductance and capacitance of the resonator L_{res} and C_{res}, respectively, as well as total capacitance C_{bank} of the capacitor bank. The negative resistance of the CCPs is designated R_{act}, R_{c} stands for the resistance of the connection from the top-level metal to the lower metal levels. The negative resistance must cancel out the losses of the oscillator. The smaller the losses are, the smaller the devices implementing the negative resistance can be, resulting in less injected noise.

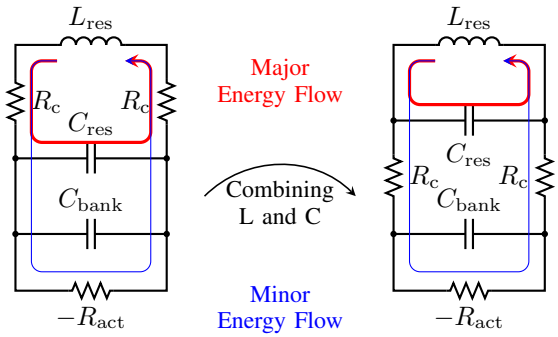

Fig. 2. Resonator model and energy flow in a standard LC-resonator (left) and the optimized design (right)

The energy flow between the inductor and the capacitors is also shown in figure 2. The major part is exchanged between the inductance and main capacitance of the resonator. In the conventional case, the current from/to these devices flows through the resistance of the interconnects, whereas in the proposed design this resistance is greatly reduced, as the capacitor and the inductor are combined on the same metal level, leading to a compact, high-Q resonator. Additionally, placing a capacitor on the same metal within the inductor removes the need for metal filling on this metal (possibly also on further levels, depending on the technology node). This increases the yield of the resonator and partly prevents quality losses due to filling.

The center frequency of the oscillator depends on the inductance and the total capacitance. The ideal approach in this case would be to remove C_{bank} and use only C_{res}, ideally resulting in less energy loss. Therefore, the more capacitance can be implemented on the top-level metal, the better the purity of the oscillator will be. For oscillators in PLLs with fixed output frequencies the required tuning range is only determined by the process spread of the center frequency of the oscillator, so the variable capacitance can be kept small.

The proposed resonator design is based on standard octagonal inductors with one winding, typical for high frequency integrated LC-oscillators, but differs from these implementations in the use of a fringe-field metal-oxide-metal capacitor (MOMCAP) on the same metal level as the inductor (figure 1). The target inductance and capacitance are 150 pH and 50 fF, respectively, resulting in a center frequency of around 60 GHz. As the minimum metal pitch of the RF metal is 1.2 µm, the capacitors on these level seem huge at first. But rough hand calculations based on parallel-plate capacitors (2) show a reasonable size which can be placed within the inductor.

$$C = \varepsilon_0\varepsilon_r \cdot N \cdot A/d = \varepsilon_0\varepsilon_r \cdot N \cdot h \cdot l/d \quad (2)$$

With a spacing d of 1.2 µm, a height h of 3 µm, a length l of 20 µm and 20 fingers, a capacitance of approximately 35 fF can be achieved (ε_r of SiO_2 = 3.9). Together with a targeted inductance of 150 pH, this equates to a center frequency of around 70 GHz, which is in the right range, especially with additional parasitics. The high capacitance density can be reached through to the high height of the top-level metals (vs.

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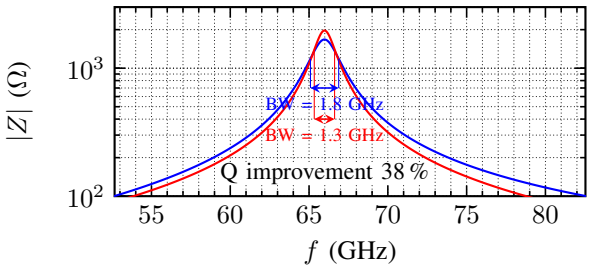

Fig. 3. Simulated resonator impedance of the optimized (red) and a regular (blue) resonator with the same resonance frequency

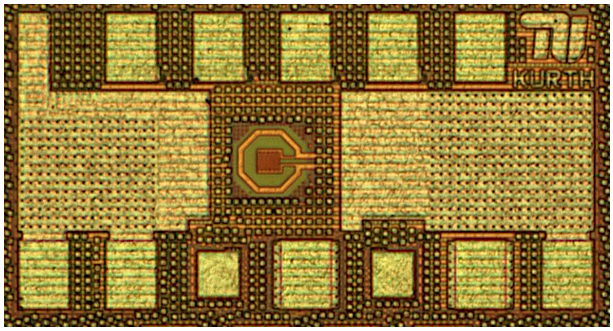

Fig. 4. Die Photograph

lower levels). Note that the actual capacitance will be higher, since this calculation vastly simplifies the actual electrical fields. The entire resonator (including the capbank and the varactor) is very compact, with an area of only $72\,\mu\text{m} \times 78\,\mu\text{m}$.

One big advantage of the combined LC-resonator is that the inductor is already filled. Density requirements often force the designer to fill the inside of inductors with metal, which lowers the quality [10]. The combined LC-resonator fully complies with all density rules without any unwanted fill metal on the three top-level metals. Lower metal levels still need to be filled, but their impact on the overall quality factor is reduced [11].

The proposed resonator was analyzed with an electromagnetic solver and compared to a conventional resonator same inductor and the corresponding capacitor on lower metals. The simulated impedance curves of both resonators are shown in figure 3 and presents an improvement of the loaded resonator-Q of over 38 % (50.8 versus 36.7).

IV. Measurement Results

The LC-oscillator was fabricated in a 22 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. The entire circuit (except for pads and their connecting wires) with serial interface, calibration of the oscillator bias current and pad/measurement instrument driver occupies $0.013\,\text{mm}^2$, whereas the oscillator core including resonator takes up only $0.007\,\text{mm}^2$. The die photograph is shown in figure 4, where the resonator and pads can be clearly seen. The control voltage of the varactor was tied to ground as the probe setup did not allow for fine tuning.

The circuit was characterized on wafer level utilizing a Rohde & Schwarz FSW67 spectrum analyzer. The measurement setup is shown in figure 5. The output signal was directly

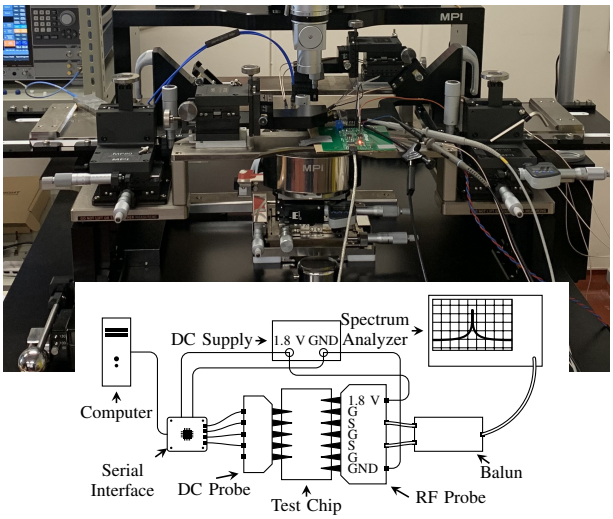

Fig. 5. Measurement Setup

probed differentially with a 67 GHz GSGSG probe and fed into a balanced-unbalanced converter (balun) to convert into a single-ended signal needed for the spectrum analyzer. The digital control (for frequency and bias current calibration) of the oscillator was performed by an auxiliary printed circuit board (PCB) for interfacing the on-chip serial interface. The measurement setup with balun, cables etc. heavily attenuates the output power of the oscillator by about 26 dB, the received power at the instrument is around −50 dBm, with −24 dBm compensated output power of the circuit. The measured spectrum of the oscillator is shown in figure 6, along with the measured phase noise spectrum. The measured coarse tuning range is shown figure 7, together with the simulated fine tuning range for every step. The oscillator shows an excellent phase noise performance of 86.5 dBc/Hz at a frequency offset of 1 MHz. The power consumption is only 4.5 mW from a single 1.8 V supply. This relates to a Figure-of-Merit (FoM) of −175 dBc/Hz. The measured total tuning range is from 47.9 GHz to 53.6 GHz (11 %).

V. Conclusion

This work presents a highly area-efficient LC-oscillator based on an optimized resonator. It was designed and fabricated in a 22 nm fully-depleted silicon-on-insulator (FDSOI) technology. The oscillator achieves a phase noise of −86.5 dBc/Hz at 1 MHz offset and a low power consumption of 4.5 mW, resulting in a Figure-of-Merit (FoM) of −175 dBc/Hz. The oscillator core occupies only an area of $0.007\,\text{mm}^2$. The comparison with recent LC-oscillators in this frequency range is shown in table 1. While other architectures achieve better phase noise results, this work excels at low power consumption and a far more compact implementation (up to $18\times$ improvement). The oscillator presented in [8] also has a very low area consumption, but the overall performance is worse and the frequency is far lower. Furthermore a starter circuit is needed to pull the circuit out of a steady state. The proposed oscillator does not need any auxiliary circuits and works from a single power supply, demonstrating a strong straight-forward design.

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Table 1. Performance Comparison with Prior-Art LC-Oscillators.

	This Work	**ISSCC'20 [7]**	**JSSC'16 [4]**	**MWC-Letters'15 [8]**
Technique	**Optimized LC-resonator**	Current-Output VCO + HCF + Current-Reuse TIA	Harmonic Extraction	Low-Q Series LC Tanks
Technology	**22 nm FDSOI CMOS**	65 nm CMOS	40 nm CMOS	40 nm CMOS
Supply Voltage (V)	**1.8**	0.9	0.7/1	0.9 – 1.1
Power Consumption (mW)	**4.5**	9.0	24.0	8.5 – 16
Output Frequency (GHz)	**53.4**	59.8	55.5	4.97
Phase Noise @ 1 MHz (dBc/Hz)	**−86.5**	−100.7	−100.1	−107
Core Area (mm^2)	**0.007**	0.12	0.13	0.0063
FoM / FoM_A @ 1 MHz (dBc/Hz)	**−175 / −166.1**	−186.7 / −165.9	−181.5 /−160	−170.1 / −162.3

$\text{FoM} = \mathcal{L}(\Delta f) - 10\log_{10}(f_0/\Delta f) + 10\log_{10}(P_{\text{DC}}/1\,\text{mW})$ $\quad \text{FoM}_\text{A} = \mathcal{L}(\Delta f) - 10\log_{10}(f_0/\Delta f) + 10\log_{10}(P_{\text{DC}}/1\,\text{mW}) + 10\log_{10}(A/1\,\text{mm}^2)$

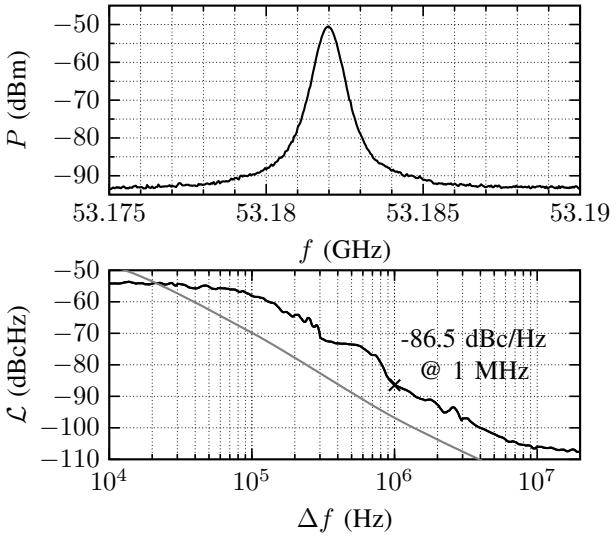

Fig. 6. Measured output power and phase noise spectrum of the oscillator. RBW = 500 kHz (power) / 10 % (phase noise), VBW = 500 kHz, Att. = 0 dB.

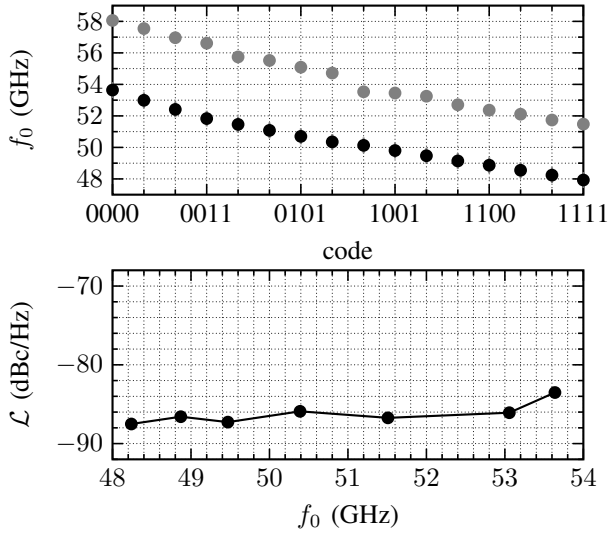

Fig. 7. Measured tuning curve of the oscillator with overlaid simulated varactor-tuning (gray). Measured phase noise at different center frequencies.

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